8 RX / 8 TX RFSoC Transceiver Board up to 6 GHz

The XCZU47DR board provides eight 14-bit ADC channels at up to 5 GSPS and eight 14-bit DAC channels at up to 9.85 GSPS. It uses SMP RF connections and dual QSFP28 interfaces for system integration.



RF conversion

Parameter	Specification
Receive channels	8
Transmit channels	8
ADC resolution	14 bit
DAC resolution	14 bit
Maximum ADC sample rate	5 GSPS
Maximum DAC sample rate	9.85 GSPS
Maximum RF frequency, RX and TX	6000 MHz
RF inputs	8 × SMP
RF outputs	8 × SMP
Digital downconversion	1 DDC / ADC
DAC interpolation factors	2×, 3×, 4×, 5×, 6×, 8×, 10×, 12×, 16×, 20×, 24×, 40×

Processing and memory

Parameter	Specification
RFSoC device	XCZU47DR-2FFVE1156I
Logic cells	930k
DSP slices	4272
Distributed RAM	13 Mbit
UltraRAM	22.5 Mbit
PS DDR4	4 GB · 64 bit · 3200 MT/s
PL DDR4 data bus	32 bit
eMMC storage	64 GB
QSPI configuration flash	2 × 2 Gbit
EEPROM	16 Kbit

System interfaces

Interface	Specification
Optical interfaces	2 × QSFP28 · 8 GTY
Ethernet	1 × RJ45 GbE
USB host	1 × USB 2.0 Type-C
Removable storage and SSD	1 × microSD / TF · 1 × M.2 M-key PCIe
Main control and I/O	J30 (J30JZLN31ZKWA000) · 4 × RS-422 · 4 × TTL IN · 4 × TTL OUT
Reserved expansion	J32 / CON34 · PZ200-2-17-W
CAN interface	CON4
FPGA debug	JTAG · 14
OCuLink	OCuLink
TTL input and output levels	3.3 / 5.0 V

Clock inputs and reference

Parameter	Specification
Clock distribution device	LMK04828
Reference clock frequency	100 MHz
Reference clock level	+10 dBm
External sampling clock frequency	3200–5000 MHz
External sampling clock level	0 dBm
Onboard system oscillator	50 MHz
External clock connector	SMP

Power and mechanical

Parameter	Specification
Supply voltage	+12 VDC
Rated supply current	≤6 A
Maximum supply ripple	≤50 mV
Power connector	J30J-9
Board dimensions	143 × 120 mm
Board weight	190 g

Connector assignments

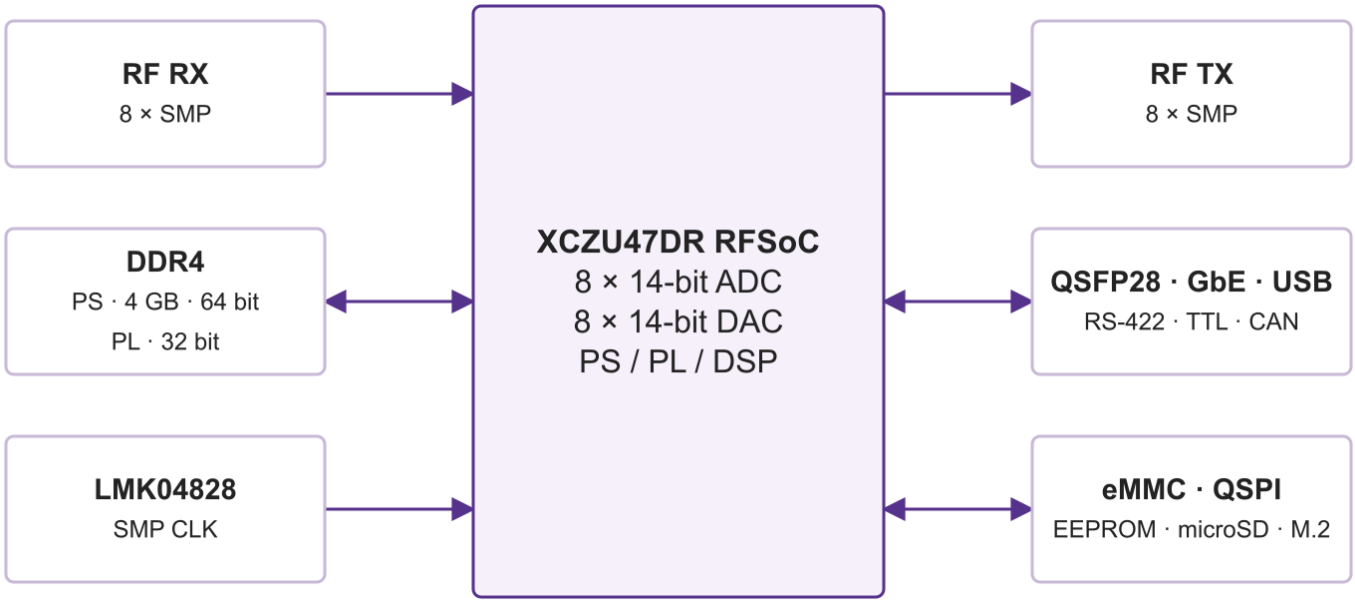
Parameter	Specification
ADC_224_VIN_0	J18
ADC_224_VIN_1	J14
ADC_225_VIN_0	J10
ADC_225_VIN_1	J7
ADC_226_VIN_0	J16
ADC_226_VIN_1	J12
ADC_227_VIN_0	J9
ADC_227_VIN_1	J5
DAC_228_VOUT_0	J19
DAC_228_VOUT_1	J15
DAC_229_VOUT_0	J11
DAC_229_VOUT_1	J6
DAC_230_VOUT_0	J17
DAC_230_VOUT_1	J13
DAC_231_VOUT_0	J8
DAC_231_VOUT_1	J4
SMP_DAC_CLK_230	J25 IN
SMP_ADC_CLK_225	J26 IN
CLK0_IN	J22 IN
CLK1_IN	J24 IN
OSCOUT / CLK2_IN	J23 I/O
J30 RS-422 0 TX+	2
J30 RS-422 0 TX−	3
J30 RS-422 0 RX+	4
J30 RS-422 0 RX−	5
J30 TTL_TX0	22
J30 TTL_RX0	27
J30 RS-422 1 TX+	7
J30 RS-422 1 TX−	8
J30 RS-422 1 RX+	9
J30 RS-422 1 RX−	10

Connector assignments

Parameter	Specification
J30 TTL_TX1	23
J30 TTL_RX1	28
J30 RS-422 2 TX+	12
J30 RS-422 2 TX−	13
J30 RS-422 2 RX+	14
J30 RS-422 2 RX−	15
J30 TTL_TX2	24
J30 TTL_RX2	29
J30 RS-422 3 TX+	17
J30 RS-422 3 TX−	18
J30 RS-422 3 RX+	19
J30 RS-422 3 RX−	20
J30 TTL_TX3	25
J30 TTL_RX3	30
J30 GND	1, 6, 11, 16, 21, 26, 31
CON4 GND	1, 4
CAN_H	2
CAN_L	3
JTAG VCC	2
JTAG TMS	4
JTAG TCK	6
JTAG TDO	8
JTAG TDI	10
JTAG GND	1, 3, 5, 7, 9, 11, 13
JTAG NC	12, 14
J30J-9 +12 V	1, 2, 3, 4
J30J-9 GND	6, 7, 8, 9

Functional block diagram

XCZU47DR RFSoC with the receive and transmit paths, clock inputs, memory and system interfaces



Document notice

Specifications are subject to revision. Before design release, confirm the current document revision and product-specific requirements with LCRF. The approved quotation and order documentation define the supplied configuration.