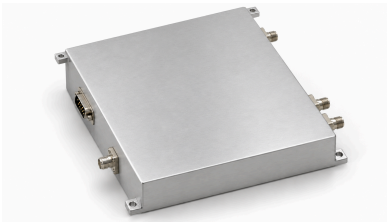


0.38–18 GHz RF Downconverter Module with Internal LO

RF downconverter covering 0.38–18 GHz with internal local oscillators, a nominal 3.75 GHz IF and up to 2 GHz instantaneous bandwidth. SPI configures the module; a separate 0.38–6 GHz output path passes RF without frequency conversion.



RF conversion performance

Parameter	Specification	Unit	Notes
RF input frequency	0.38–18	GHz	Broadband RF input
Converted IF output band	3.75 ±1	GHz	Nominal centre 3.75 GHz
Direct RF output band	0.38–6	GHz	Separate output path without frequency conversion
Instantaneous bandwidth	Up to 2	GHz	Source description; converted IF operation
Conversion gain — LNA path	60 typical	dB	LNA path
Conversion gain — Through Path	25 minimum	dB	Source-defined low-gain condition; not the direct RF output
Noise figure — LNA path	4 typical	dB	LNA path
Noise figure — Through Path	10 typical	dB	Through Path; not the direct RF output
Output 1 dB compression point	≥+12	dBm	OP1dB
Output third-order intercept	≥+25	dBm	OIP3

Programmable attenuation

Parameter	Specification	Unit
RF attenuation range	31.5 (6-bit)	dB
RF attenuation step	0.5	dB
IF attenuation range	31.5 (6-bit)	dB
IF attenuation step	0.5	dB
IF calibration attenuation range	15.5 (5-bit)	dB
IF calibration attenuation step	0.5	dB

Spurious and rejection performance

Parameter	Specification	Unit	Notes
Absolute spurious level	≤−87	dBm	Equivalent RF input power; 2000 MHz bandwidth
Spurious-free dynamic range	≥55	dB	Pin = −25 dBm; low-gain path test
Harmonic suppression	≥45	dB	Pin = −29 dBm; low-gain path test
Image rejection	≥70	dB	-
Gain flatness	≤5	dB	Across the specified operating range
IF rejection	≥50	dBc	At 3.75 GHz ±1500 MHz

Internal LO tuning · Source design guarantees apply only where identified.

Parameter	Specification	Unit	Notes
LO1 operating frequency	24–40	GHz	Design guaranteed
LO1 frequency step	10	MHz	-
LO1 switching response time	≤100	μs	Design guaranteed
LO2 output frequencies	18.25 / 25.75	GHz	Design guaranteed; discrete alternatives

LO1 phase-noise design targets · Designed to meet; not measured results.

Parameter	Specification	Unit	Notes
LO1 phase noise at 100 Hz	≤−65	dBc/Hz	Design target; not a measured result
LO1 phase noise at 1 kHz	≤−80	dBc/Hz	Design target; not a measured result
LO1 phase noise at 10 kHz	≤−88	dBc/Hz	Design target; not a measured result
LO1 phase noise at 100 kHz	≤−90	dBc/Hz	Design target; not a measured result
LO1 phase noise at 1 MHz	≤−100	dBc/Hz	Design target; not a measured result

LO2 phase-noise design targets · Designed to meet; not measured results.

Parameter	Specification	Unit	Notes
LO2 phase noise at 100 Hz	≤−75	dBc/Hz	Design target; not a measured result
LO2 phase noise at 1 kHz	≤−85	dBc/Hz	Design target; not a measured result
LO2 phase noise at 10 kHz	≤−90	dBc/Hz	Design target; not a measured result
LO2 phase noise at 100 kHz	≤−93	dBc/Hz	Design target; not a measured result
LO2 phase noise at 1 MHz	≤−103	dBc/Hz	Design target; not a measured result

RF interfaces

Parameter	Specification	Unit	Notes
RF port	SMA	-	RF input
IF port	SMA	-	IF output
BITE port	SMA	-	Built-in test and calibration
REF port	SMA	-	100 MHz reference signal output

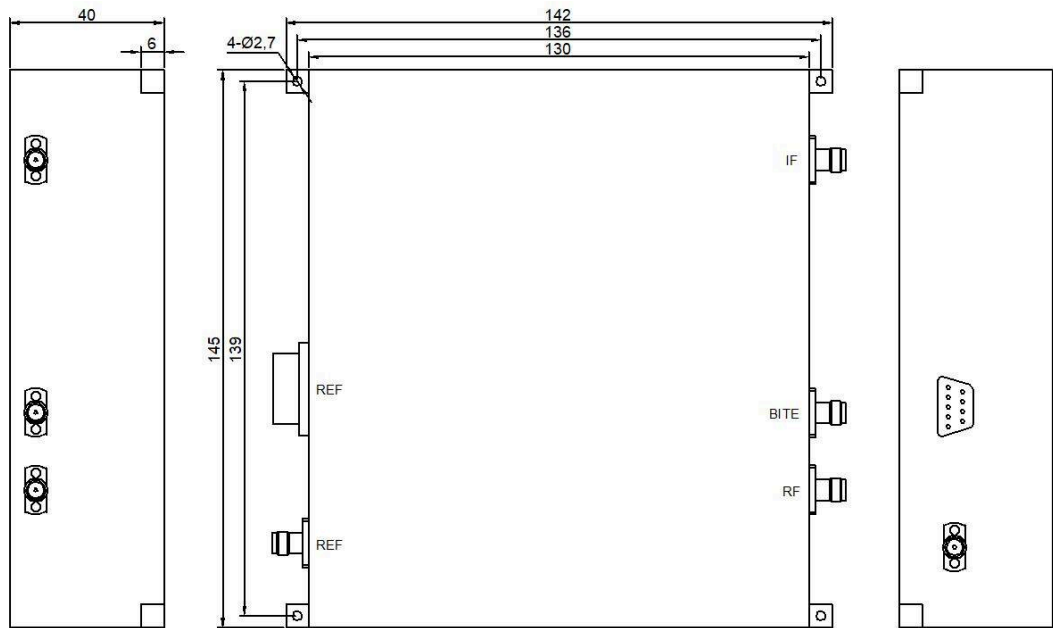
Power and SPI pin assignments · J30J-9ZKP; source pin numbering.

Parameter	Specification	Unit	Notes
Pin 1	+12 V	-	DC power input
Pin 2	+12 V	-	DC power input
Pin 3	GND	-	Power ground
Pin 4	GND	-	Power ground
Pin 5	SCK	-	SPI clock
Pin 6	CSB	-	SPI chip select
Pin 7	MOSI	-	SPI data input
Pin 8	MISO	-	SPI data output
Pin 9	NC	-	Reserved

Preliminary mechanical specifications · Preliminary. Table and drawing disagree; confirm the installation envelope.

Parameter	Specification	Unit	Notes
Length	145	mm	Preliminary; installation dimensions require confirmation
Width	142	mm	Preliminary; drawing/body/tab dimensions disagree
Height	40	mm	Preliminary
Overall dimensions	145 ×142 ×40	mm	Preliminary; source says excluding mounting lugs; drawing conflict unresolved
RF connectors	Four SMA connectors	-	Preliminary mechanical table
Power/control connector	Side-mounted J30J series	-	Preliminary; pin table identifies J30J-9ZKP

Mechanical Outline



All dimensions are in mm [in].

Current publication record

1.0 · 2026-10-05. First publication of approved product data.

Product overview

LCMIXUD-380-18000-2G integrates RF switching, a low-noise amplifier, a switched filter bank and two stages of frequency conversion. Its 0.38–18 GHz RF input is translated to a nominal 3.75 GHz IF, with a specified 3.75 GHz ±1 GHz output band and up to 2 GHz instantaneous bandwidth. Signals from 0.38 to 6 GHz can instead use an output path that bypasses frequency conversion. The conversion specifications distinguish an LNA path, with 60 dB typical gain and 4 dB typical noise figure, from the source-defined Through Path, with 25 dB minimum gain and 10 dB typical noise figure. Through Path is the low-gain condition within the signal chain; these values are not assigned to the separate direct RF output. RF and IF attenuation each extend to 31.5 dB in 0.5 dB steps, while IF calibration attenuation extends to 15.5 dB. The module integrates internal LO1 and LO2. The crystal-oscillator reference is divided into a branch used within the module and another branch providing the 100 MHz REF output. The source identifies the LO1

frequency range and switching response, and the two LO2 output frequencies, as design guarantees. The 10 MHz LO1 frequency step has no such qualification. The two phase-noise tables are design targets, not measured performance reports. The main image is a structural illustration constrained by the source outline, not a product photograph. The mechanical table is preliminary and does not agree fully with the drawing: 145×142×40 mm is stated excluding mounting lugs, whereas the drawing shows a 142 mm span across the tabs, a 130 mm body width and 136 mm hole spacing. The installation envelope requires engineering confirmation.

Interfaces and system integration

The four SMA ports are RF input, IF output, BITE test/calibration and REF reference output. LO1 and LO2 are internal sources, not external LO input ports. The functional diagram distinguishes the low-gain route around the LNA from the output switch that selects converted IF or the direct 0.38–6 GHz RF path. The power/control connector is J30J-9ZKP. Pins 1 and 2 carry +12 V, pins 3 and 4 are GND, and pins 5–8 are SCK, CSB, MOSI and MISO respectively; pin 9 is NC/reserved. SPI controls the major functions, but register addresses, frame format, mode and timing are not specified in the supplied document. The spurious limit is referred to equivalent RF input power over 2000 MHz bandwidth. SFDR and harmonic suppression are given under low-gain test conditions at –25 dBm and –29 dBm input power respectively. Those conditions remain attached to the values and do not establish performance for the direct RF output. Before an installation drawing or cable assembly is released, confirm the conflicting mounting envelope and connector mating details. SMA gender/impedance, supply tolerance/current, operating temperature and environmental qualification are not established by this source.

Document notice

Specifications are subject to revision. Before design release, confirm the current document revision and product-specific requirements with LCRF. The approved quotation and order documentation define the supplied configuration.