2–18 GHz SPI-Controlled Broadband RF Downconverter Module



This broadband RF downconverter translates 2–18 GHz input signals to a fixed 1.8 GHz IF output for receiver, signal-monitoring, analysis and test systems. A switched RF filter bank precedes a two-stage frequency-conversion chain supplied by external LO1 and LO2 inputs.

SPI control selects one of seven overlapping RF filters, switches between the RF and BITE calibration inputs, and sets separate RF and calibration attenuators in 0.5 dB steps. RF attenuation extends to 31.5 dB; calibration attenuation extends to 15.5 dB. The specified ±0.5 dB gain variation requires calibration by the user.

Conversion gain is at least 28 dB and noise figure is at most 12 dB. The output-referred 1 dB compression point is at least 12 dBm, and OIP3 is at least 25 dBm. The source gives separate conditions for spurious, SFDR, harmonic and filter rejection; each is retained beside the corresponding specification.

The aluminum housing measures 87×70×13.5 mm with four Ø2.7 mm mounting holes. Supply voltage is +12 VDC typical and current is 320 mA typical. The main image is a structural illustration based on the mechanical outline, not a product photograph; the original dimensioned drawing remains the installation reference.

RF conversion performance

Parameter	Specification	Unit
RF input frequency [1]	2–18	GHz
IF output centre frequency [2]	1.8	GHz
Conversion gain [3]	≥28	dB
Noise figure	≤12	dB
Gain variation [4]	±0.5	dB
Output 1 dB compression point [5]	≥12	dBm
Output third-order intercept point [6]	≥25	dBm
RF attenuation range [7]	31.5	dB
Calibration attenuation range [8]	15.5	dB
Internal spurious [9]	≤−90	dBm
Single-tone SFDR [10]	≥55	dB
Harmonic rejection [11]	≥45	dB
Image rejection	≥70	dB
Gain flatness [12]	≤5	dB
IF filter rejection [13]	≥50	dBc

[1] Broadband
[2] Fixed
[3] Minimum
[4] User calibrated

[5] OP1dB
[6] OIP3
[7] 0.5 dB steps; 6 bits
[8] 0.5 dB steps; 5 bits
[9] Equivalent RF input power; 1000 MHz bandwidth
[10] Pin = −25 dBm
[11] Pin = −29 dBm
[12] 1 GHz bandwidth
[13] At 1.8 GHz ±700 MHz

Power and environmental limits

Parameter	Specification	Unit
Supply voltage	+12 (Typical)	VDC
Supply current	320 (Typical)	mA
Operating temperature	−40 to +70	°C
Storage temperature	−55 to +125	°C

RF and LO interfaces

Interface	Specification	Unit
RF input [1]	RF	-
Calibration signal input [2]	BITE	-
First external LO input [3]	LO1: 22–40	GHz
Second external LO input [3]	LO2: 20.2	GHz
IF output [4]	IF: 1.8	GHz

[1] 2–18 GHz input
[2] User gain calibration
[3] Input power −3 to +3 dBm
[4] Fixed centre frequency

Power and SPI pin assignments

Parameter	Specification
Power positions 1–2 [1]	+12 V
Power positions 3–4 [2]	GND
SPI position 1 [3]	SPI_MOSI
SPI position 2 [4]	SPI_SCK
SPI position 3 [5]	SPI_NSS

Power and SPI pin assignments

Parameter	Specification
SPI position 4 [2]	GND

[1] Input
[2] Ground
[3] Data
[4] Clock
[5] LE

SPI control frame

Parameter	Specification	Unit
Control rate [1]	2 / 10	Mbps
Frame header [2]	AA 55 (hexadecimal)	-
Control word [3]	Data[15:0]	-
Frame ending [2]	44 BB (hexadecimal)	-
Power-down control state [4]	Data[15:0] = 0	-

[1] Typical / maximum
[2] Two bytes
[3] Two bytes; byte order not defined in source
[4] All data bits must be zero when powering down

Control-word bit assignments

Parameter	Specification
Bits 15, 14, 13 [1]	C2, C1, C0
Bit 12 [2]	EN
Bit 11 [3]	RF@BITE
Bits 10–5 [4]	RF ATT
Bits 4–0 [5]	Cal ATT

[1] RF filter selection; defined codes listed below
[2] 1: power up; 0: power down
[3] 1: BITE calibration path; 0: RF path
[4] Bits 10/9/8/7/6/5: 16/8/4/2/1/0.5 dB; 1 enables each step, 0 disables
[5] Bits 4/3/2/1/0: 8/4/2/1/0.5 dB; 1 enables each step, 0 disables

Switched RF filter bank

Parameter	Specification	Unit
C2:C1:C0 = 000	1.9–3.2 (Filter passband; product RF range starts at 2 GHz)	GHz
C2:C1:C0 = 001	2.2–3.7	GHz
C2:C1:C0 = 010	2.7–4.6	GHz
C2:C1:C0 = 011	3.6–6.1	GHz
C2:C1:C0 = 100	5.1–8.9	GHz
C2:C1:C0 = 101	7.9–13.8	GHz
C2:C1:C0 = 110	12.8–18 (Code 111 is not defined in the source)	GHz

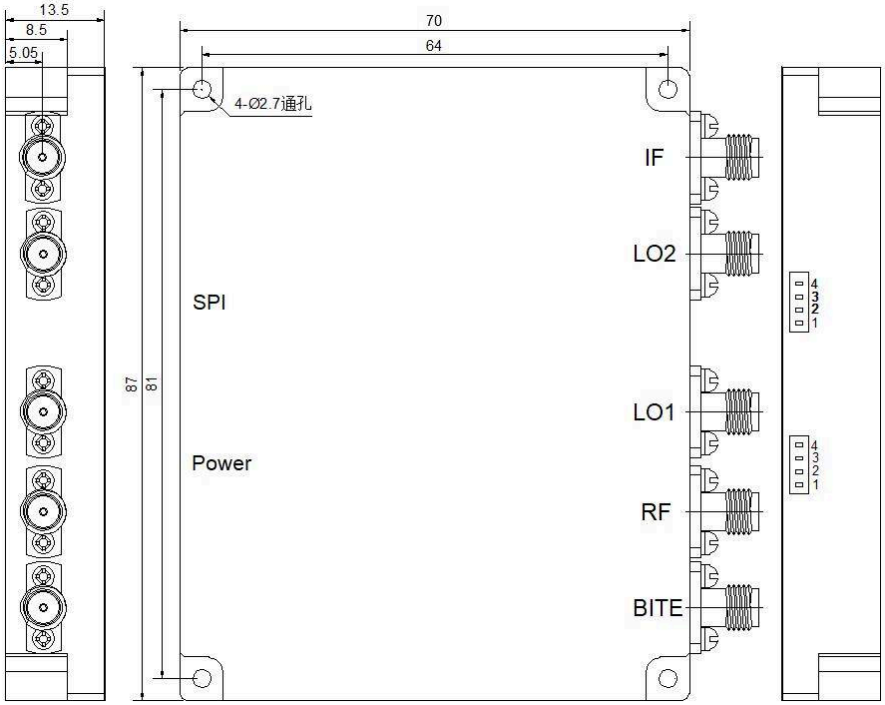
Mechanical outline

Parameter	Specification	Unit
Housing dimensions [1]	87×70×13.5	mm
Mass	≤500	g
Mounting holes [2]	4×Ø2.7	mm
Mounting-hole centres [3]	81×64	mm

[1] Excludes connector protrusions

[2] Through-holes

[3] Along the 87 mm and 70 mm housing edges respectively



Product overview

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Interfaces and system integration

LO1 accepts 22–40 GHz and LO2 accepts 20.2 GHz; each specified input power range is −3 to +3 dBm. These are external inputs. The functional diagram shows a 22 GHz first IF filter and a final 1.8 GHz ±500 MHz IF filter; the fixed 1.8 GHz specification is the IF centre frequency, not a 1.8 GHz-wide bandwidth. The RF and BITE paths share the conversion chain. Bit 11 selects the BITE path for user gain calibration or the RF path for signal reception. Filter codes cover overlapping sub-bands, and the 1.9 GHz lower edge of the first filter does not extend the specified 2 GHz RF operating limit. The SPI frame consists of 0xAA 0x55, a two-byte Data[15:0] control word, and 0x44 0xBB. Maximum control rate is 10 Mbps and typical rate is 2 Mbps. When powering down the module, all control data bits must be set to zero. The source does not define byte order, SPI mode or timing margins; these require engineering confirmation before writing a controller driver. The pin-assignment table preserves the source-defined positions for power and SPI. Connector part numbers and complete physical pin counts require engineering confirmation before making a harness. Allow for coaxial connector protrusions and cable clearance beyond the housing dimensions.

Document notice

Specifications are subject to revision. Before design release, confirm the current document revision and product-specific requirements with LCRF. The approved quotation and order documentation define the supplied configuration.