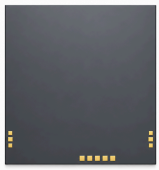
8500–10500 MHz 4-Bit GaAs MMIC Digital Time Delay Die

LCI-TTD-8500-10500-4B is a 4-bit GaAs pHEMT digital time-delay bare die for 8500–10500 MHz, integrating delay paths and a parallel TTL control driver.

Time delay: 52.7 ps (typical) (T1; t_nom = 52 ps); Time delay: 416 ps (typical) (T4; t_nom = 416 ps); Insertion loss: 12 dB (typical) / 13 dB (maximum). Die dimensions: 4 × 4.2 × 0.1 mm.



RF characteristics

TA = +25 °C; VEE = -5 V

Parameter	Symbol	Minimum	Typical	Maximum	Value	Unit
Operating frequency	-	8500	-	10500	-	MHz
Insertion loss	-	-	12	13	-	dB
Time delay (T1)	-	-	52.7	-	T1; t_nom = 52 ps	ps
Time delay (T2)	-	-	102	-	T2; t_nom = 104 ps	ps
Time delay	-	-	212	-	T3; t_nom = 208 ps	ps
Time delay	-	-	416	-	T4; t_nom = 416 ps	ps
Delay-induced amplitude variation	-	-	±0.3	-	-	dB
Input VSWR	-	-	1.3	-	-	-
Output VSWR	-	-	1.3	-	-	-

DC bias and current

TA = +25 °C

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Negative supply voltage	-	-5.3	-5	-4.7	V
Negative-supply quiescent current	-	-	0.003	-	A
Input drive current [1]	-	-	0.2	-	mA
High-level input voltage	-	3	-	5	V
Low-level input voltage	-	0	-	0.4	V

[1] VIH = +5 V; TTL

Absolute limits

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Minimum negative supply voltage	-	-6	-	-	V
Input drive current	-	-	-	0.3	mA
Maximum input power	-	-	-	25	dBm

Environmental specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Storage temperature	-	-65	-	150	°C
Operating temperature	-	-55	-	85	°C

Bond-pad assignments

Pins	Symbol	Function	Notes
1, 3, 4, 6	GND	Ground; no wire bond required	-
2	RF1	RF port	1
5	RF2	RF port	2
11	VEE	DC bias	−5 V
7	T1	Delay control	0.5λ; TTL
8	T2	Delay control	λ; TTL
9	T3	Delay control	2λ; TTL
10	T4	Delay control	4λ; TTL

Control truth table

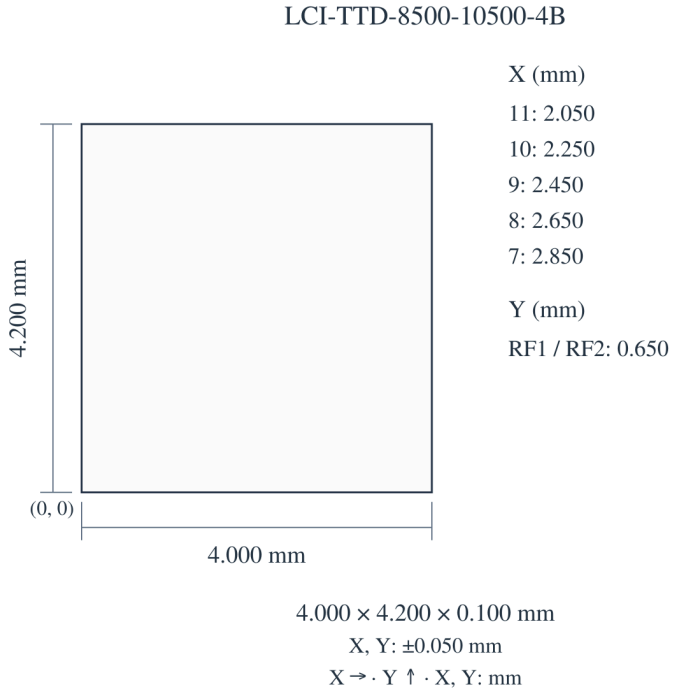
0 = 0 V; 1 = +5 V

State	T1	T2	T3	T4
Reference state	0	0	0	0
0.5λ (52 ps)	1	0	0	0
λ (104 ps)	0	1	0	0
2λ (208 ps)	0	0	1	0
4λ (416 ps)	0	0	0	1

Die dimensions

Parameter	Value	Unit
Die dimensions	4 × 4.2 × 0.1	mm

Reference drawing showing selected dimensions in mm. Use complete drawings for fabrication and wire bonding.



Current publication record · 1.6 · 2026-11-12. Product description or editorial content updated. Replaces revision 1.5.

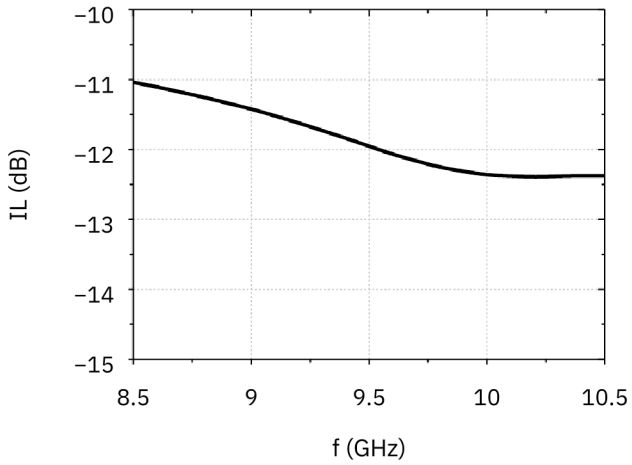
Die integration and bias sequencing

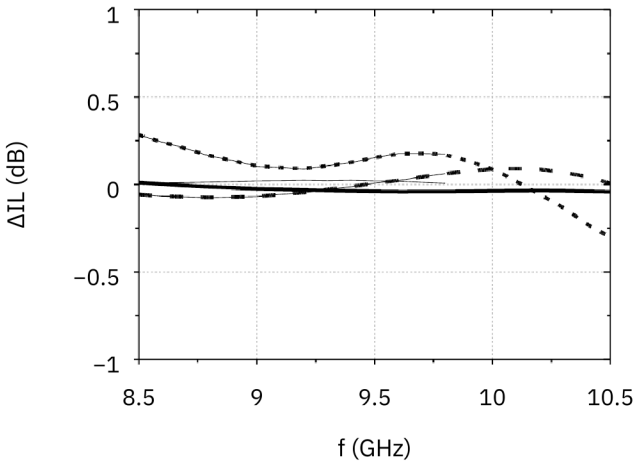
Control interface: Parallel TTL control.

Performance curves

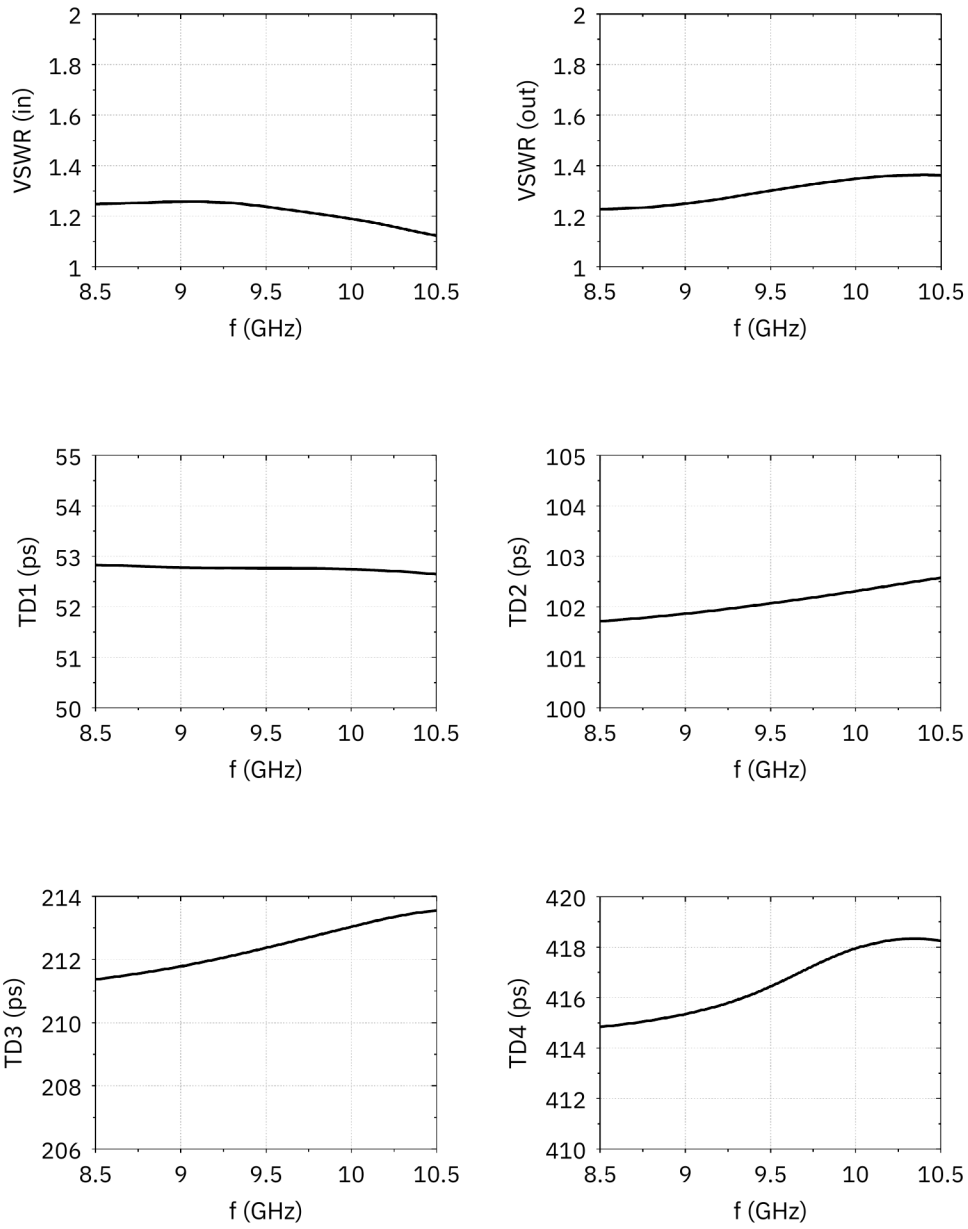
Read each figure with its stated operating conditions.

Insertion loss; Delay-induced amplitude variation.





Input matching; Output matching; Delay accuracy.



Document notice

Specifications are subject to revision. Before design release, confirm the current document revision and product-specific requirements with LCRF. The approved quotation and order documentation define the supplied configuration.