9000–10000 MHz GaN T/R MMIC Power Amplifier Die

LCI-TRPA-9000-10000-PS35T-M is a GaN MMIC power amplifier supplied as bare die for 9000–10000 MHz. It supports pulsed operation. The die integrates a transmit power-amplifier path and a switched receive bypass path.

PSAT: 35 dBm (typical); Power gain: 21 dB (typical); PAE: 35 % (typical). Die dimensions: 2.1 × 1.5 × 0.1 mm.



RF characteristics

TA = +25 °C; Vd = +28 V; Vg = -2.6 V

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating frequency	f	9000	-	10000	MHz
Saturated output power	Psat	-	35	-	dBm
Power gain	Gp	-	21	-	dB
Power-gain flatness	ΔGp	-	-	±0.2	dB
Power-added efficiency	PAE	-	35	-	%
Small-signal gain	S21	-	30	-	dB
Small-signal gain flatness	ΔS21	-	-	±0.5	dB
Input VSWR	VSWR(in)	-	1.2	1.5	-

DC bias and current

TA = +25 °C

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain operating voltage	Vd	-	28	-	V
Gate operating voltage	Vg	-3	-2.6	-2.2	V
Quiescent drain current	Id	-	0.1	-	A
Dynamic drain current	Idd	-	0.3	-	A
Dynamic gate current	Igg	-	0.5	1	mA

Absolute limits

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Maximum drain-source voltage	Vd	-	-	28	V
Minimum gate bias	Vg	-5	-	-	V
Maximum input power	Pin	-	-	18	dBm
Storage temperature	TSTG	-65	-	150	°C
Maximum channel temperature	Top	-	-	225	°C

Die dimensions

Parameter	Value	Unit
Die dimensions	2.1 × 1.5 × 0.1	mm

Current publication record · 1.8 · 2026-11-12. Product description or editorial content updated. Replaces revision 1.7.

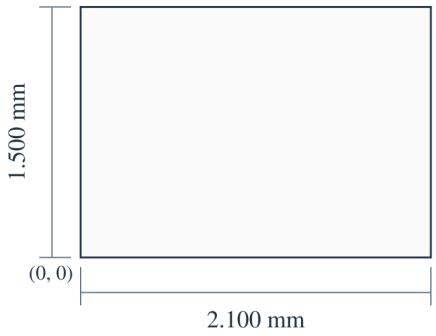
Die integration and bias sequencing

Integrated DC blocking: RFin / RFout. DC path to ground: RFout → GND. Transmit state: Tin → Tout; Vd = +28 V; Vg = -2.6 V; V1 = 0 V; V2 = +28 V. Receive state: Rin → Rout; Vd = +28 V; Vg = -5 V; V1 = +28 V; V2 = 0 V. Apply gate bias before drain bias. Remove drain bias before gate bias.

Mechanical Outline

Outline and dimensioned coordinates in mm. Use this drawing as a dimensional reference. Fabrication and wire bonding require complete drawings.

LCI-TRPA-9000-10000-PS35T-M



X, Y (mm)
1 Tin: (0.110, 1.085)
2 Vg: (0.130, 0.120)
3 Vd1: (0.835, 0.180)
4 Vd2: (0.990, 0.140)
5 V1: (1.800, 0.140)
6 V2: (1.950, 0.140)
7 Tout/Rin: (1.900, 1.085)
8 Rout: (1.490, 1.280)

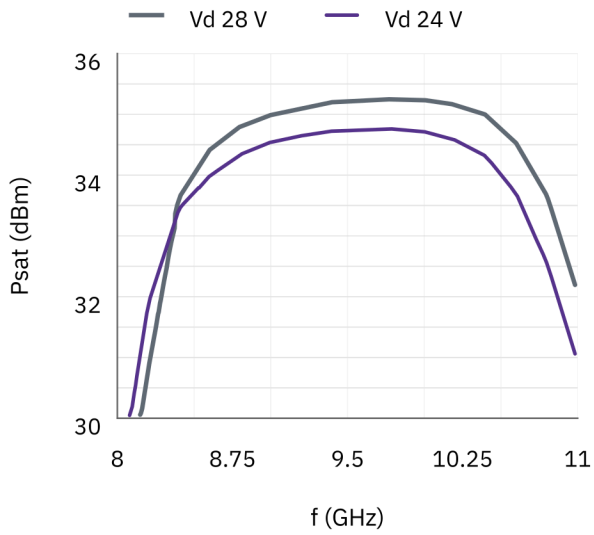
2.100 × 1.500 × 0.100 mm
X, Y: ±0.100 mm
X → · Y ↑ · X, Y: mm

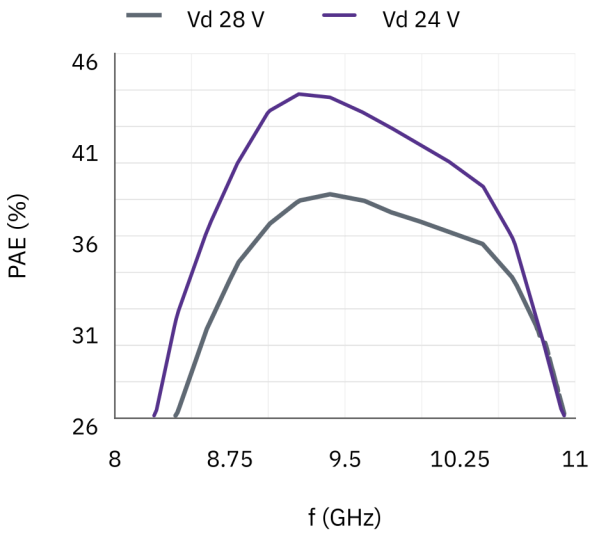
Performance curves

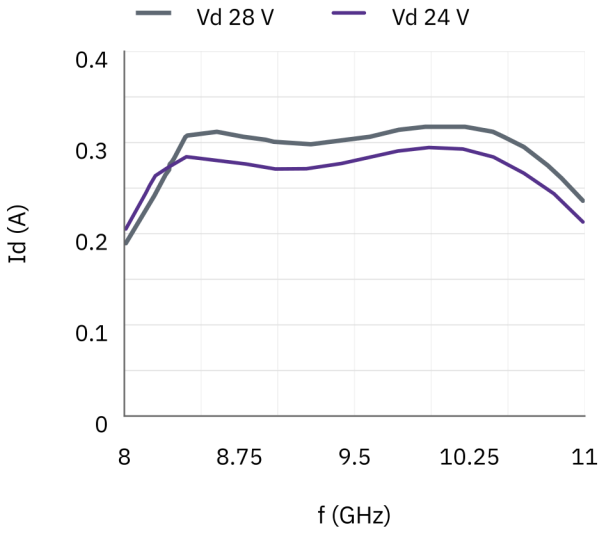
Each performance plot applies to its stated operating conditions.

Pulsed — Power-added efficiency; Saturated output power; Dynamic drain current.

Figure notes: TA=+25°C; Vg=-2.6V. Readings are approximate. Pulse width = 100 µs; duty cycle = 10%. V1 = 0 V; V2 = 28 V; Pin = 14 dBm; Vd = 28 / 24 V.

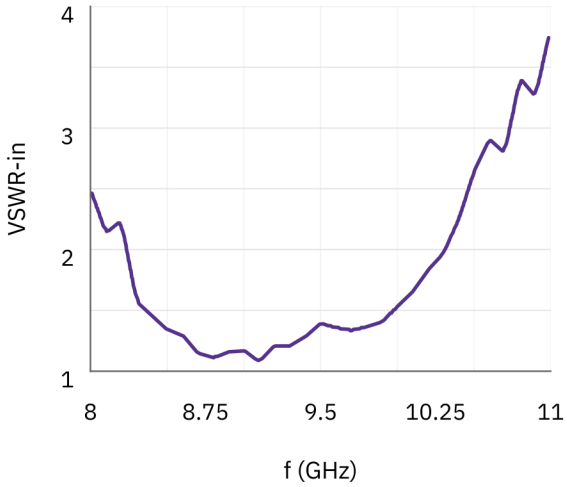


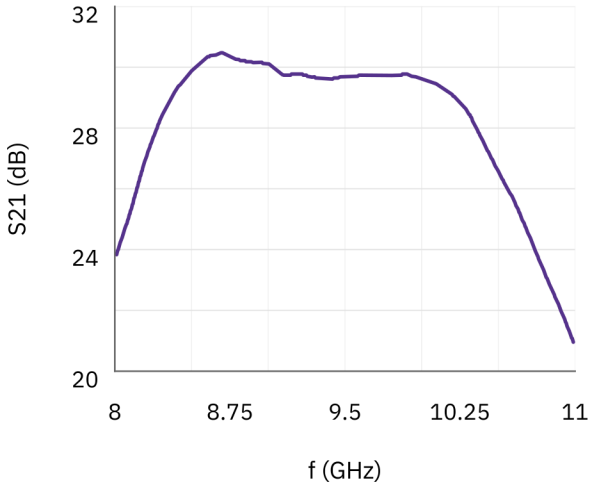




Tx — Input matching; Gain.

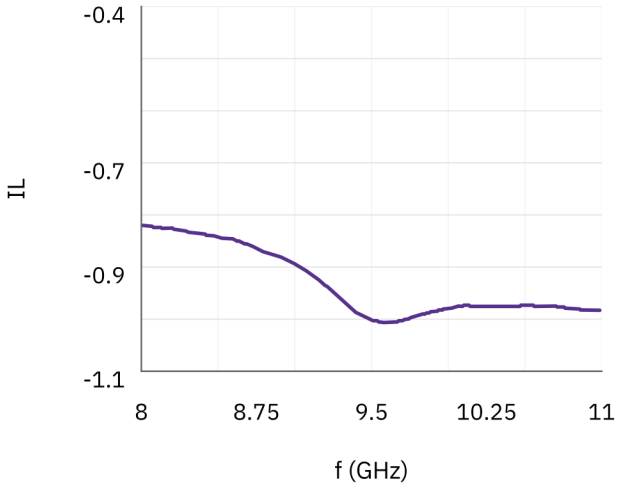
Figure notes: TA=+25°C; Vd=+28V; Vg=-2.6V. Readings are approximate. Pin = −10 dBm; V1 = 0 V; V2 = 28 V.

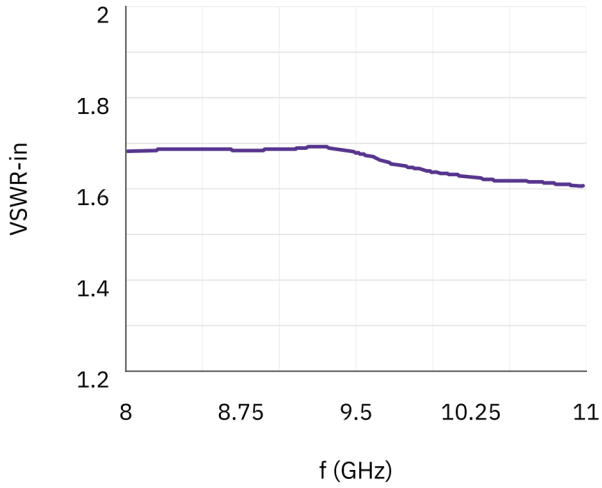


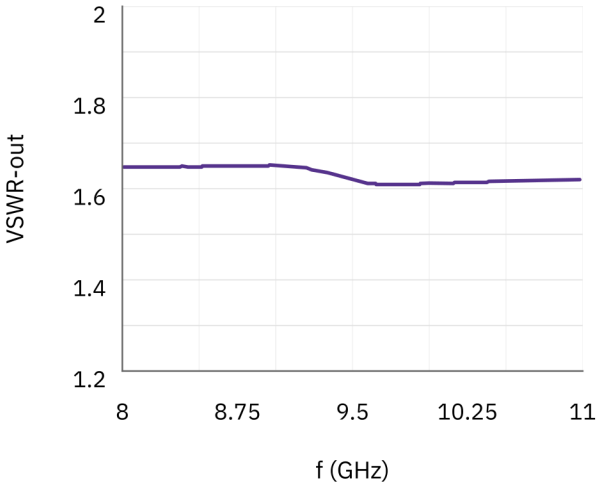


Rx — Pulsed — Insertion loss; Input matching; Output matching.

Figure notes: TA=+25°C; Vd=+28V; Vg=-5V. Readings are approximate. Pulse width = 100 µs; duty cycle = 10%. Pin = −10 dBm; V1 = 28 V; V2 = 0 V. The IL axis has no specified unit. Do not read its values as dB.







Document notice

Specifications are subject to revision. Before design release, confirm the current document revision and product-specific requirements with LCRF. The approved quotation and order documentation define the supplied configuration.