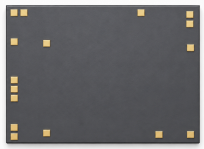
8000–12000 MHz GaN T/R MMIC Power Amplifier Die

LCI-TRPA-8000-12000-PS41T-M is a GaN MMIC power amplifier supplied as bare die for 8000–12000 MHz. It supports pulsed operation. The die integrates a transmit power-amplifier path and a switched receive bypass path.

PSAT: 41 dBm (typical); Power gain: 25 dB (typical); PAE: 38 % (typical). Die dimensions: 3.2 × 2.3 × 0.1 mm.



RF characteristics

TA = +25 °C; Vd = +28 V; Vg = -2.6 V

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating frequency	f	8000	-	12000	MHz
Saturated output power	Psat	-	41	-	dBm
Power gain	Gp	-	25	-	dB
Power-gain flatness	ΔGp	-	-	±0.5	dB
Power-added efficiency	PAE	-	38	-	%
Small-signal gain	S21	-	35	-	dB
Small-signal gain flatness	ΔS21	-	-	±0.5	dB
Input VSWR	VSWR(in)	-	1.8	2	-

DC bias and current

TA = +25 °C

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain operating voltage	Vd	-	28	-	V
Gate operating voltage	Vg	-3	-2.6	-2.4	V
Quiescent drain current	Id	-	0.6	-	A
Dynamic drain current	Idd	-	1.1	1.3	A
Dynamic gate current	Igg	-	3	10	mA

Absolute limits

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Maximum drain-source voltage	Vd	-	-	28	V
Minimum gate bias	Vg	-5	-	-	V
Maximum input power	Pin	-	-	20	dBm
Storage temperature	TSTG	-65	-	150	°C
Maximum channel temperature	Top	-	-	225	°C

Die dimensions

Parameter	Value	Unit
Die dimensions	3.2 × 2.3 × 0.1	mm

Current publication record · 1.8 · 2026-11-12. Product description or editorial content updated. Replaces revision 1.7.

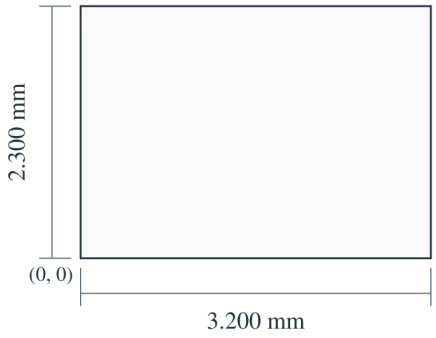
Die integration and bias sequencing

Integrated DC blocking: RFin / RFout. DC path to ground: RFout → GND. Transmit state: Tin → Tout; Vd = +28 V; Vg = -2.6 V; V1 = -28 V; V2 = 0 V. Receive state: Rin → Rout; Vd = +28 V; Vg = -5 V; V1 = 0 V; V2 = -28 V. Apply gate bias before drain bias. Remove drain bias before gate bias.

Mechanical Outline

Outline and dimensioned coordinates in mm. Use this drawing as a dimensional reference. Fabrication and wire bonding require complete drawings.

LCI-TRPA-8000-12000-PS41T-M



X, Y (mm)
1 Tin: (0.110, 0.910)
2 Vg: (0.110, 0.110)
3 Vd1/Vd2: (0.650, 0.170)
4 Vd3: (2.540, 0.140)
5 V1: (3.070, 0.140)
6 V2: (3.050, 1.600)
7 Tout/Rin: (3.030, 2.146)
8 Rout: (0.120, 2.180)
9 V2: (2.240, 2.180)

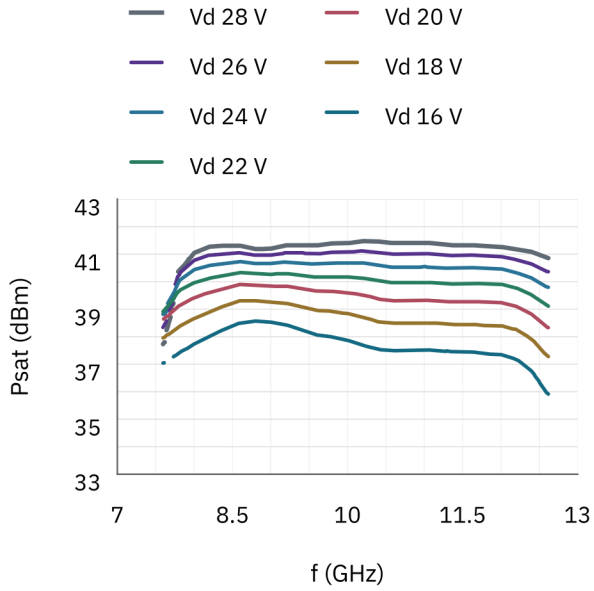
3.200 × 2.300 × 0.100 mm
X, Y: ±0.100 mm
X → · Y ↑ · X, Y: mm

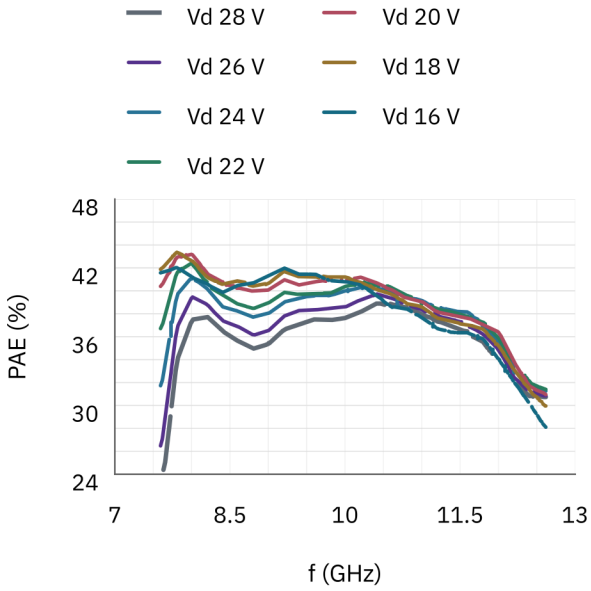
Performance curves

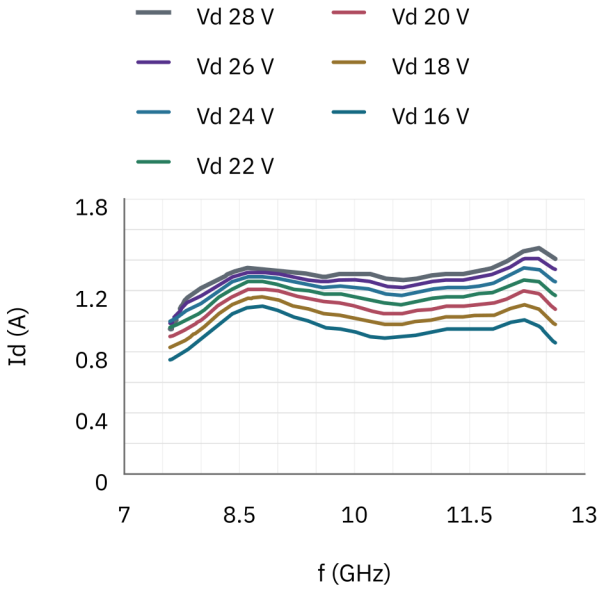
Each performance plot applies to its stated operating conditions.

Pulsed — Saturated output power; Power-added efficiency; Dynamic drain current.

Figure notes: TA=+25°C; Vg=-2.6V. Readings are approximate. Pulse width = 100 µs; duty cycle = 10%. V1 = −Vd; V2 = 0 V; Pin = 16 dBm; Vd = 28 / 26 / 24 / 22 / 20 / 18 / 16 V.

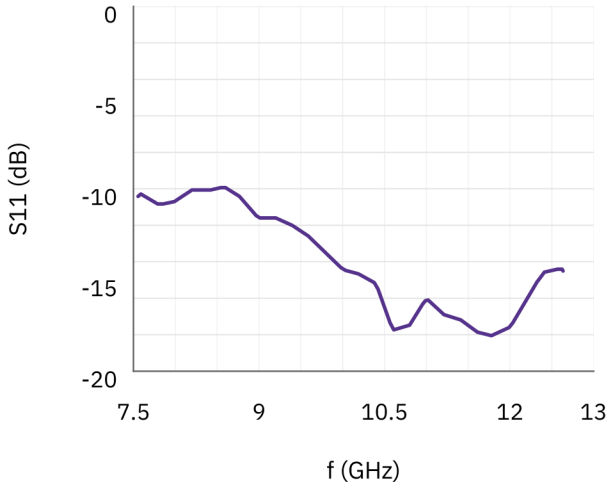


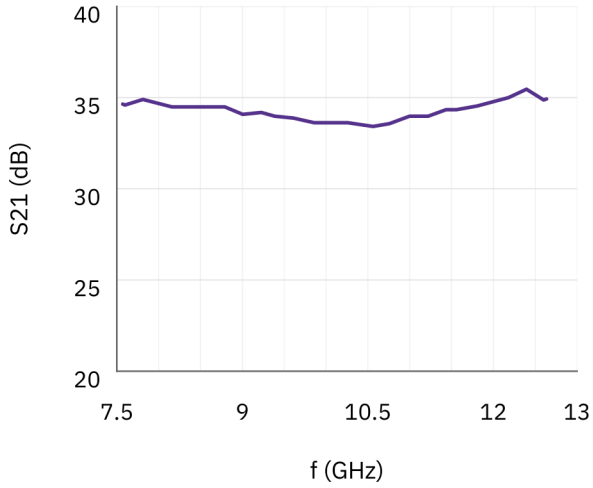




Tx — S11 (dB); S21 (dB).

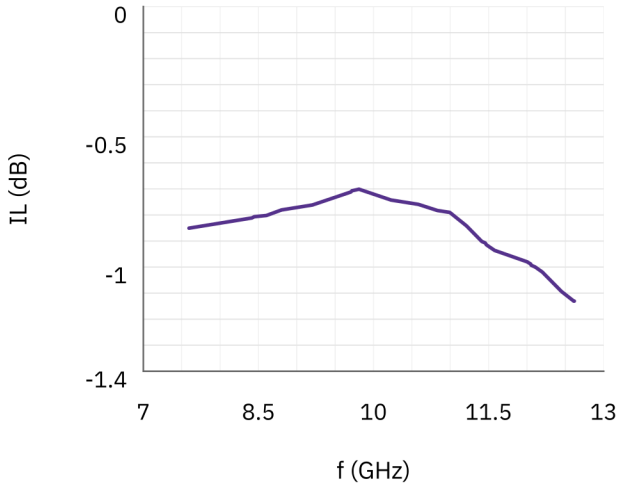
Figure notes: TA=+25°C; Vd=+28V; Vg=-2.6V. Readings are approximate. Pin = −10 dBm; V1 = −28 V; V2 = 0 V. Input matching is plotted as dB(S11).

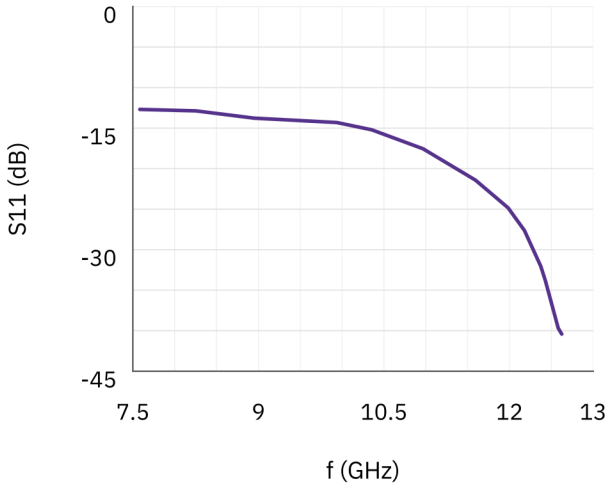


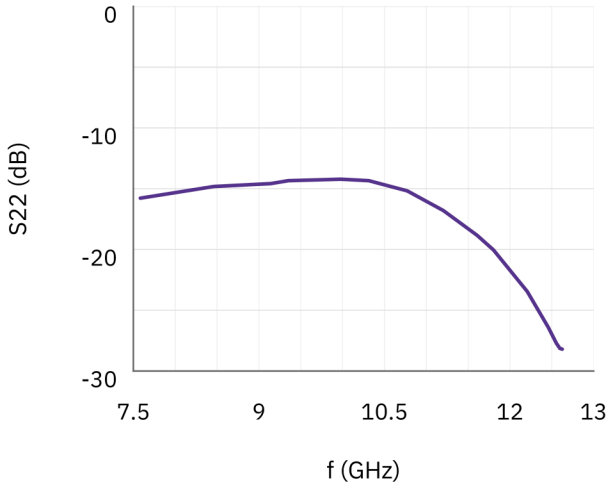


Rx — Pulsed — Insertion loss; S11 (dB); S22 (dB).

Figure notes: TA=+25°C; Vd=+28V; Vg=-5V. Readings are approximate. Pin = −10 dBm; V1 = 0 V; V2 = −28 V. Input and output matching are plotted as dB(S11) and dB(S22), respectively.







Document notice

Specifications are subject to revision. Before design release, confirm the current document revision and product-specific requirements with LCRF. The approved quotation and order documentation define the supplied configuration.