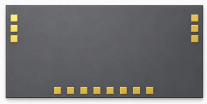
5000–6000 MHz 6-Bit GaAs MMIC Digital Phase Shifter Die

LCI-PS-5000-6000-6B is a 6-bit GaAs pHEMT digital phase-shifter bare die for 5000–6000 MHz, providing stepped RF phase control.

RMS phase error: 1 ° (typical); Insertion loss: 7 dB (typical); Phase shift range: 5.625 ° (minimum) / 354.375 ° (maximum). Die dimensions: 3.1 × 1.5 × 0.1 mm.



RF characteristics

TA = +25 °C; VEE = -5 V

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating frequency	-	5000	-	6000	MHz
Insertion loss	-	-	7	-	dB
Phase shift range	-	5.625	-	354.375	°
RMS phase error	-	-	1	-	°
Phase-induced amplitude variation	-	-	-	±0.5	dB
Input VSWR	-	-	1.2	-	-
Output VSWR	-	-	1.2	-	-

DC bias and current

TA = +25 °C

Parameter	Symbol	Minimum	Typical	Maximum	Value	Unit
Negative supply voltage	-	-5.3	-5	-4.7	-	V
Negative-supply quiescent current	-	-	0.002	-	-	A
Input drive current	-	-	0.2	-	VIH = +5 V; TTL	mA
High-level input voltage	-	4	-	5	-	V
Low-level input voltage	-	0	-	0.4	-	V
Phase step	-	-	-	-	5.625	°

Absolute limits

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Minimum negative supply voltage	-	-6	-	-	V
Input drive current	-	-	-	0.3	mA
Maximum input power	-	-	-	20	dBm

Environmental specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Storage temperature	-	-65	-	150	°C
Operating temperature	-	-55	-	85	°C

Bond-pad assignments

Pins	Symbol	Function	Notes
1, 3, 4, 6	GND	Ground; no wire bond required	-
2	RF1	RF port	1
5	RF2	RF port	2
7, 14	VEE	DC bias	–5 V
8	P6	Phase control	180°; TTL
9	P5	Phase control	90°; TTL
10	P4	Phase control	45°; TTL
11	P3	Phase control	22.5°; TTL
12	P2	Phase control	11.25°; TTL
13	P1	Phase control	5.625°; TTL

Control truth table

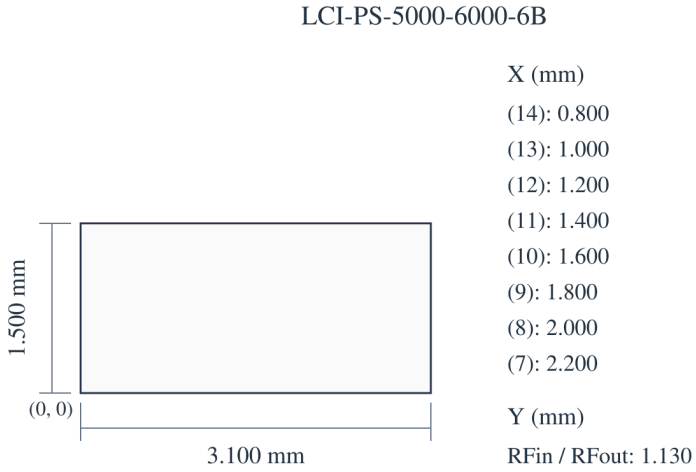
H = +5 V; L = 0 V

State	P1	P2	P3	P4	P5	P6
Reference state	L	L	L	L	L	L
5.625°	H	L	L	L	L	L
11.25°	L	H	L	L	L	L
22.5°	L	L	H	L	L	L
45°	L	L	L	H	L	L
90°	L	L	L	L	H	L
180°	L	L	L	L	L	H

Die dimensions

Parameter	Value	Unit
Die dimensions	3.1 × 1.5 × 0.1	mm

Partial dimensional reference in mm. Fabrication and wire bonding require complete drawings.



Current publication record · 1.6 · 2026-11-12. Product description or editorial content updated. Replaces revision 1.5.

Die integration and bias sequencing

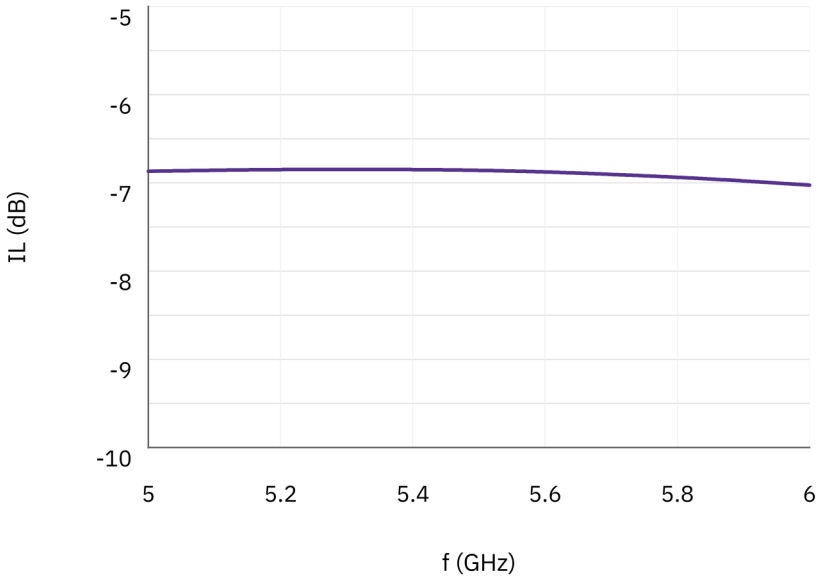
Control interface: Parallel TTL control.

Performance curves

Each performance plot applies to its stated operating conditions.

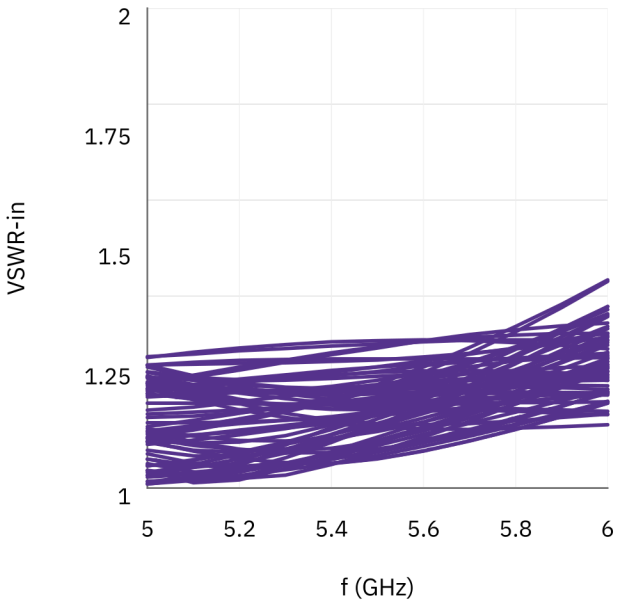
Insertion loss.

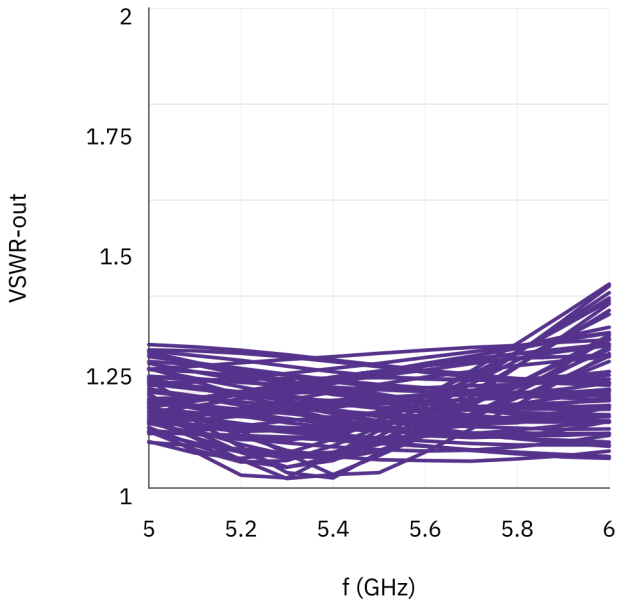
Readings are approximate.

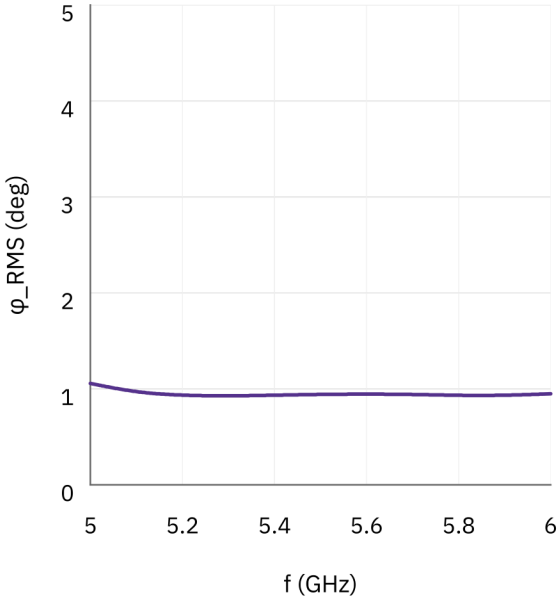


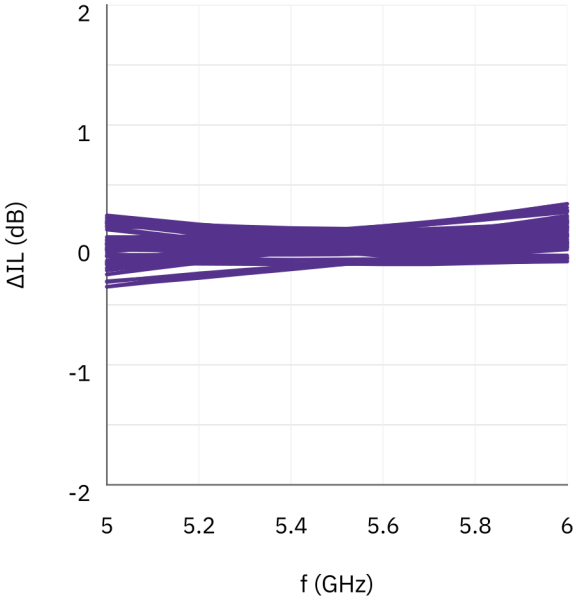
Input matching; Output matching; RMS phase error; Phase-induced amplitude variation.

Readings are approximate.









Document notice

Specifications are subject to revision. Before design release, confirm the current document revision and product-specific requirements with LCRF. The approved quotation and order documentation define the supplied configuration.