14000–18000 MHz 6-Bit GaAs MMIC Digital Phase Shifter Die

LCI-PS-14000-18000-6B-D is a 6-bit GaAs pHEMT digital phase-shifter bare die for 14000–18000 MHz, providing stepped RF phase control.

RMS phase error: 1.2 ° (typical); Insertion loss: 7 dB (typical); Phase shift range: 5.625 ° (minimum) / 354.375 ° (maximum). Die dimensions: 2.5 × 1.3 × 0.1 mm.



RF characteristics

TA = +25 °C

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating frequency	-	14000	-	18000	MHz
Insertion loss	-	-	7	-	dB
Phase shift range	-	5.625	-	354.375	°
RMS phase error	-	-	1.2	-	°
Phase-induced amplitude variation	-	-	±0.3	-	dB
Input VSWR	-	-	1.5	-	-
Output VSWR	-	-	1.3	-	-

DC bias and current

Parameter	Symbol	Minimum	Typical	Maximum	Value	Unit
Negative-supply quiescent current	-	-	0.003	-	-	A
Negative supply voltage	-	-	-	-	-5	V
Control voltage	-	-	-	-	0 / +5	V
Phase step	-	-	-	-	5.625	°

Absolute limits

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Minimum negative supply voltage	-	-6	-	-	V
Maximum control voltage	-	-	-	6	V
Input drive current	-	-	-	0.3	mA
Maximum input power	-	-	-	25	dBm

Environmental specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Storage temperature	-	-65	-	150	°C
Operating temperature	-	-55	-	85	°C

Bond-pad assignments

Pins	Symbol	Function	Notes
1, 3, 4, 6	GND	Ground; no wire bond required	-
2	RF_1	RF port	1
5	RF_2	RF port	2
7	P6	Phase control	180°; 0 / +5 V
8	P5	Phase control	90°; 0 / +5 V
9	P4	Phase control	45°; 0 / +5 V
10	P3	Phase control	22.5°; 0 / +5 V
11	P2	Phase control	11.25°; 0 / +5 V
12	P1	Phase control	5.625°; 0 / +5 V
13	VE	DC bias	–5 V

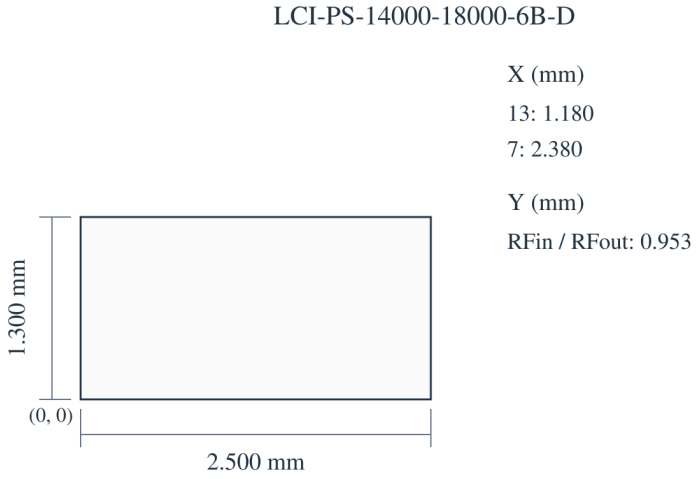
Control truth table

State	P1	P2	P3	P4	P5	P6
Reference state	0 V	0 V	0 V	0 V	0 V	0 V
5.625°	5 V	0 V	0 V	0 V	0 V	0 V
11.25°	0 V	5 V	0 V	0 V	0 V	0 V
22.5°	0 V	0 V	5 V	0 V	0 V	0 V
45°	0 V	0 V	0 V	5 V	0 V	0 V
90°	0 V	0 V	0 V	0 V	5 V	0 V
180°	0 V	0 V	0 V	0 V	0 V	5 V

Die dimensions

Parameter	Value	Unit
Die dimensions	2.5 × 1.3 × 0.1	mm

Reference drawing showing selected dimensions in mm. Use complete drawings for fabrication and wire bonding.



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Die integration and bias sequencing

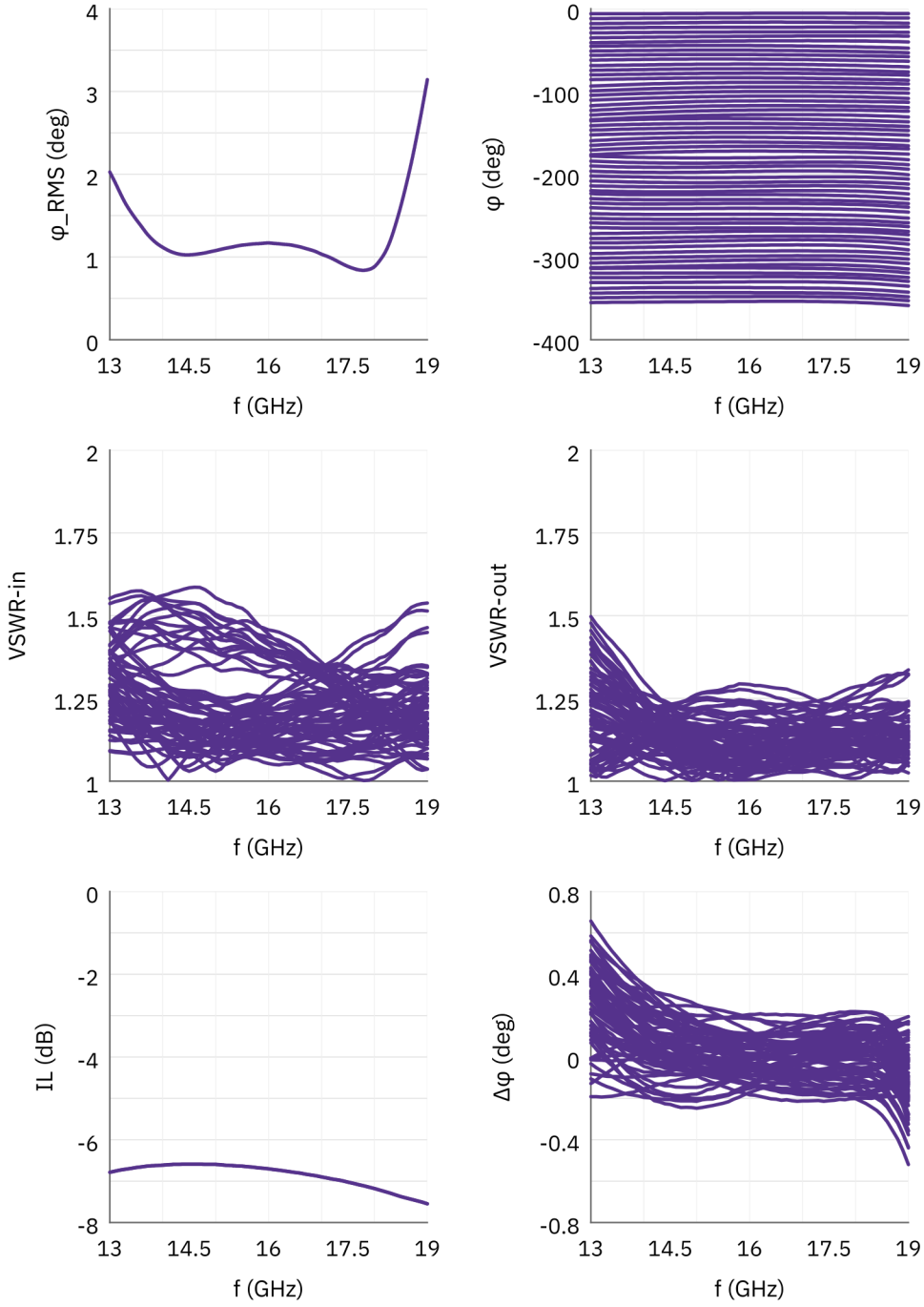
Control interface: Parallel TTL control.

Performance curves

Read each figure with its stated operating conditions.

Insertion loss; Input matching; Output matching; Phase shift; RMS phase error; ΔPHS.

Readings are approximate. Read the final plot by its vertical axis, delta_PHS (deg), which shows phase variation in degrees.



Document notice

Specifications are subject to revision. Before design release, confirm the current document revision and product-specific requirements with LCRF. The approved quotation and order documentation define the supplied configuration.