# 8500–10500 MHz GaN MMIC Power Amplifier Die

LCI-PA-8500-10500-PS52T is a GaN MMIC power amplifier supplied as bare die for 8500–10500 MHz. It supports pulsed operation.

The RF table specifies: Saturated output power: 52 dBm (typical); Power gain: 24 dB (typical); Power-added efficiency: 45 % (typical). RF test conditions: TA = +25 °C; Vd = +48 V; Vg = -2.6 V. Die dimensions: 3.9 × 6.5 × 0.1 mm.



## RF characteristics

TA = +25 °C; Vd = +48 V; Vg = -2.6 V

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Operating frequency | f | 8500 | - | 10500 | MHz |
| Saturated output power | Psat | - | 52 | - | dBm |
| Power gain | Gp | - | 24 | - | dB |
| Power-gain flatness | ΔGp | - | - | ±0.5 | dB |
| Power-added efficiency | PAE | - | 45 | - | % |
| Small-signal gain | S21 | - | 34 | - | dB |
| Small-signal gain flatness | ΔS21 | - | - | ±1 | dB |
| Input VSWR | VSWR(in) | - | 1.6 | 2 | - |

## DC bias and current

TA = +25 °C

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Drain voltage | Vd | - | 48 | 50 | V |
| Gate voltage | Vg | -3 | -2.6 | -2.4 | V |
| Quiescent drain current | Id | - | 3.3 | - | A |
| Dynamic drain current | Idd | - | 7 | 7.5 | A |
| Dynamic gate current | Igg | - | 3 | 10 | mA |

## Absolute limits

Absolute limits; these are not normal operating targets.

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Maximum drain-source voltage | Vd | - | - | 50 | V |
| Minimum gate bias | Vg | -5 | - | - | V |
| Maximum channel temperature | Top | - | - | 225 | °C |
| Storage temperature | TSTG | -65 | - | 150 | °C |

## Die dimensions

| Parameter | Value | Unit |
|---|---|---|
| Die dimensions | 3.9 × 6.5 × 0.1 | mm |
| Plan-view outline tolerance | ±100 (Plan-view outline only; the source does not specify thickness tolerance.) | µm |

**Current publication record** · 1.8 · 2026-11-12. Product description or editorial content updated. Replaces revision 1.7.

## Die integration and bias sequencing

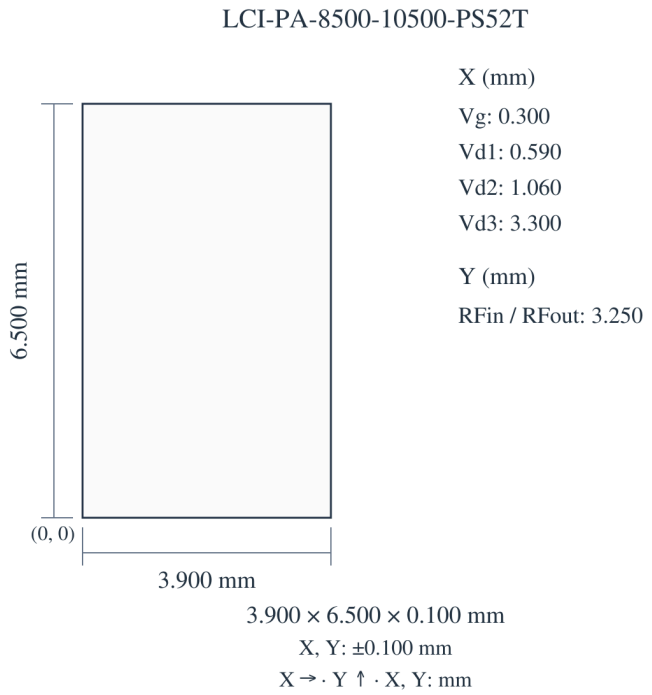
Apply gate bias before drain bias at power-up. At power-down, remove drain bias before gate bias. Use clean handling, ESD protection and a carrier with thermal expansion compatible with the SiC die.

## Bond-pad dimensions

Symbol: RFin; Dimensions (µm): 100 × 100. Symbol: Vg; Dimensions (µm): 120 × 100. Symbol: Vd1; Dimensions (µm): 120 × 100. Symbol: Vd2; Dimensions (µm): 120 × 100. Symbol: Vd3; Dimensions (µm): 250 × 100. Symbol: RFout; Dimensions (µm): 100 × 120.

## Mechanical Outline

Outline and dimensioned coordinates in mm. Use this drawing as a dimensional reference. Fabrication and wire bonding require complete drawings.

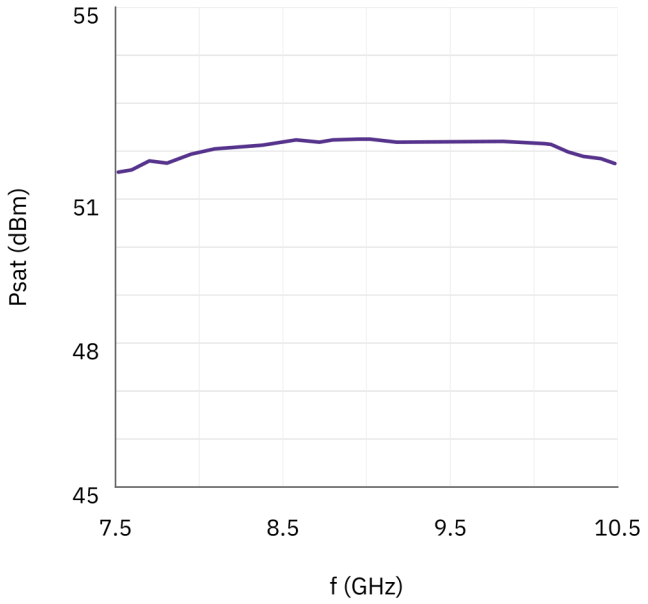


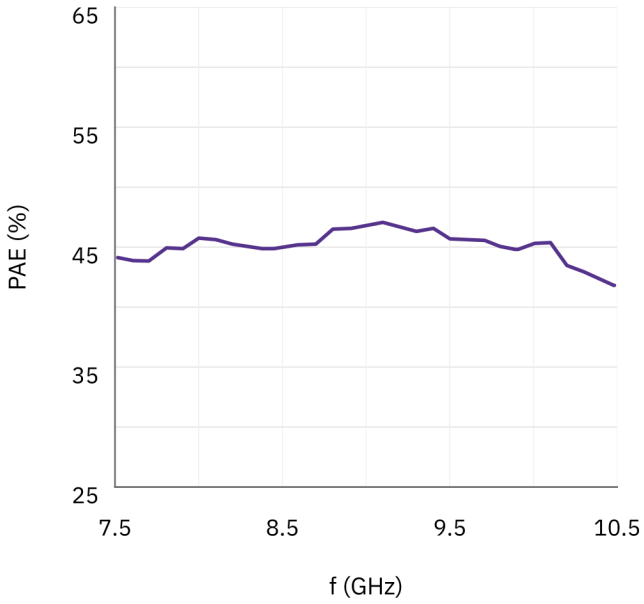
## Performance curves

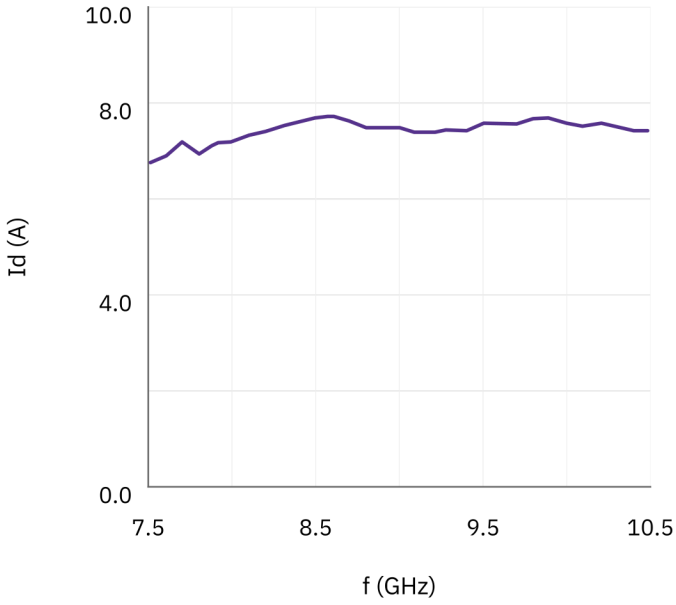
Each performance plot applies to its stated operating conditions.

**Saturated output power; Power-added efficiency; Dynamic drain current.**

Figure notes: TA=25°C; Vd=+48V; Vg=-2.6V; Pin=28dBm. Readings are approximate.




**Document notice**

Specifications are subject to revision. Before design release, confirm the current document revision and product-specific requirements with LCRF. The approved quotation and order documentation define the supplied configuration.