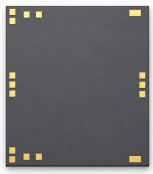
# 8000–9400 MHz GaN MMIC Power Amplifier Die

LCI-PA-8000-9400-PS45T-A is a GaN MMIC power amplifier supplied as bare die for 8000–9400 MHz. It supports CW and pulsed operation.

The RF table specifies: Saturated output power: 45 dBm (typical); Power gain: 31 dB (typical); Power-added efficiency: 52 % (typical). RF test conditions: TA = +25 °C; Vd = +28 V; Vg = -1.8 V. Die dimensions: 3 × 3.2 × 0.1 mm.



## RF characteristics

TA = +25 °C; Vd = +28 V; Vg = -1.8 V

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Operating frequency | f | 8000 | - | 9400 | MHz |
| Saturated output power | Psat | - | 45 | - | dBm |
| Power gain | Gp | - | 31 | - | dB |
| Power-gain flatness | ΔGp | - | - | ±0.5 | dB |
| Power-added efficiency | PAE | - | 52 | - | % |
| Small-signal gain | S21 | - | 37 | - | dB |
| Small-signal gain flatness | ΔS21 | - | - | ±1 | dB |
| Input VSWR | VSWR(in) | - | 1.6 | 2 | - |

## DC bias and current

TA = +25 °C

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Drain voltage | Vd | - | 28 | 32 | V |
| Gate voltage | Vg | -2.6 | -1.8 | -1.6 | V |
| Quiescent drain current | Id | - | 1.7 | - | A |
| Dynamic drain current | Idd | - | 2.5 | 2.7 | A |
| Dynamic gate current | Igg | - | 0.2 | 1 | mA |

## Absolute limits

Absolute limits; these are not normal operating targets.

| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Maximum drain-source voltage | Vd | - | - | 32 | V |
| Minimum gate bias | Vg | -5 | - | - | V |
| Maximum input power | Pin | - | - | 20 | dBm |
| Maximum channel temperature | Top | - | - | 225 | °C |
| Storage temperature | TSTG | -65 | - | 150 | °C |

## Die dimensions

| Parameter | Value | Unit |
|---|---|---|
| Die dimensions | 3 × 3.2 × 0.1 | mm |
| Plan-view outline tolerance | ±100 (Plan-view outline only; the source does not specify thickness tolerance.) | µm |

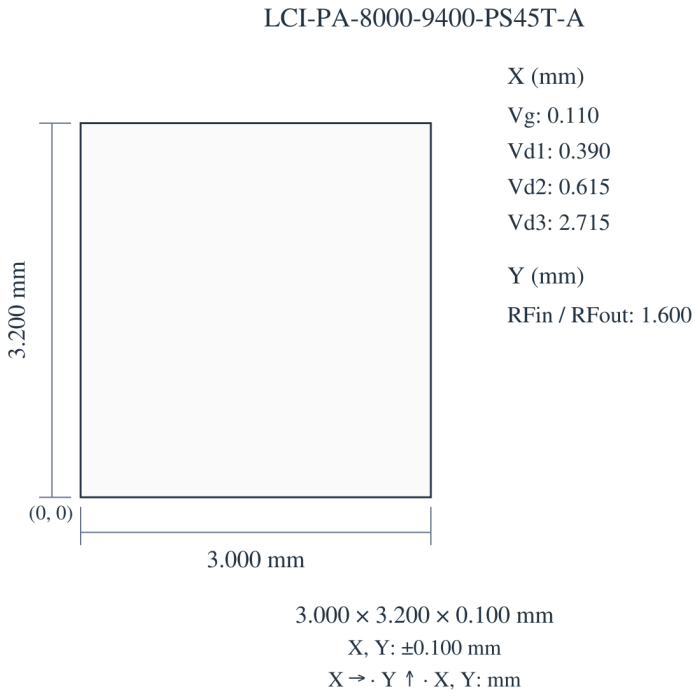
**Current publication record** · 1.8 · 2026-11-12. Product description or editorial content updated. Replaces revision 1.7.

## Die integration and bias sequencing

Apply gate bias before drain bias at power-up. At power-down, remove drain bias before gate bias. Use clean handling, ESD protection and a carrier with thermal expansion compatible with the SiC die.

## Mechanical Outline

Outline and dimensioned coordinates in mm. Use this drawing as a dimensional reference. Fabrication and wire bonding require complete drawings.

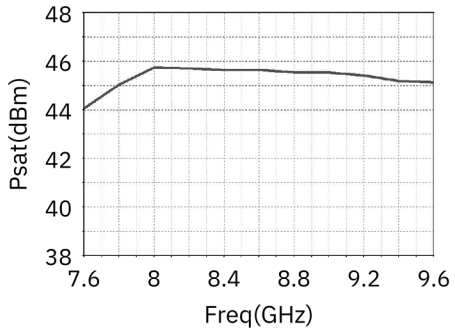


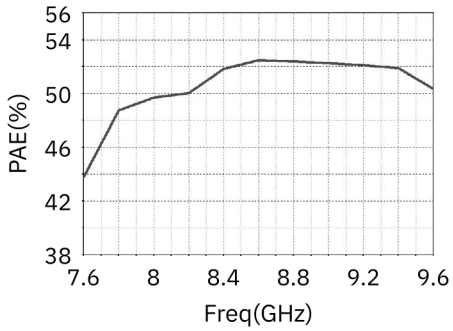
## Performance curves

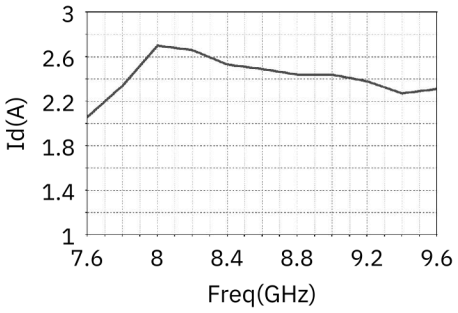
Each performance plot applies to its stated operating conditions.

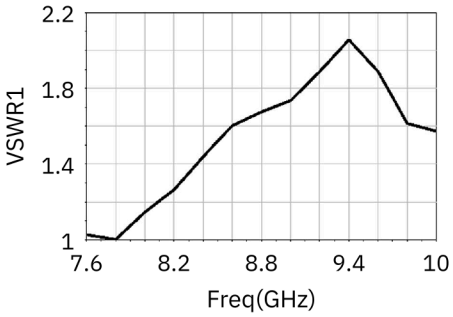
**Pulsed — Saturated output power; Power-added efficiency; Dynamic drain current; Input matching; Gain.**

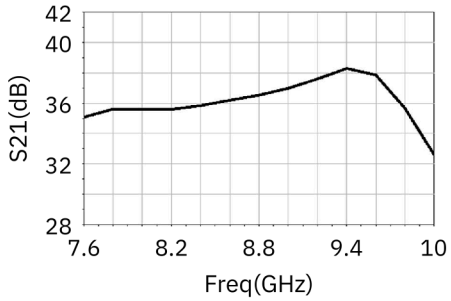
Figure notes: TA=+25°C; Vd=+28V; Vg=-1.8V.  PW = 100 µs; D = 10%. Plots 1–3: Pin = 14 dBm. Plots 4–5: Pin = -10 dBm.



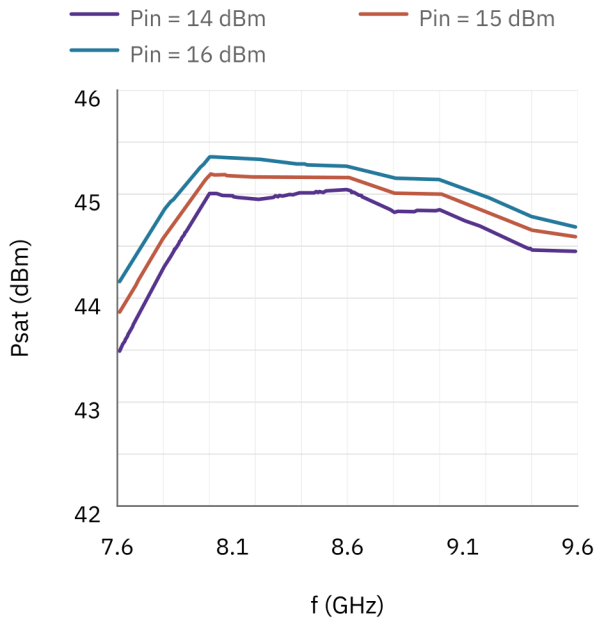



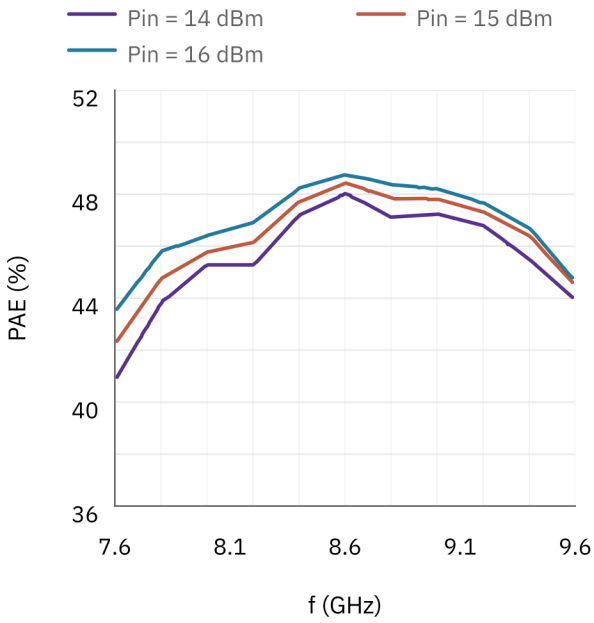



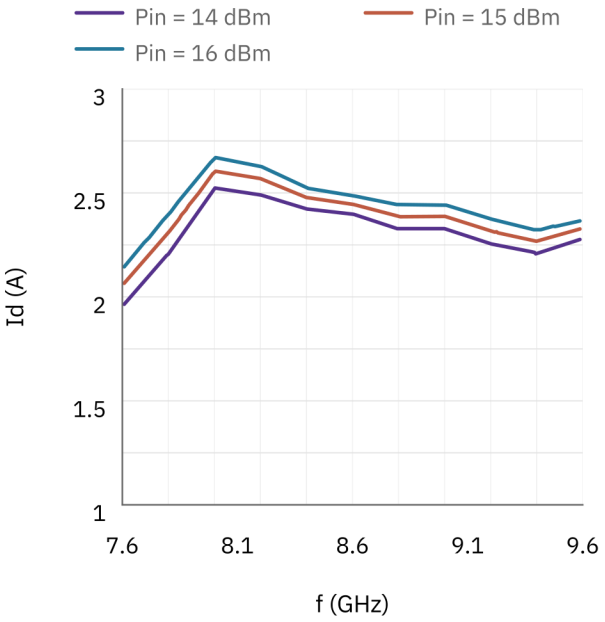



### Continuous wave (CW) — Saturated output power; Power-added efficiency; Dynamic drain current.

Figure notes: TA=+25°C; Vd=+28V; Vg=-1.8V. Readings are approximate. Pin = 14 / 15 / 16 dBm. Read each trace with the conditions shown in its plot.




**Document notice**

Specifications are subject to revision. Before design release, confirm the current document revision and product-specific requirements with LCRF. The approved quotation and order documentation define the supplied configuration.