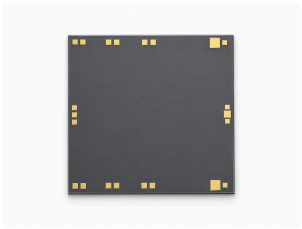
11500–18000 MHz GaN MMIC Power Amplifier Die

LCI-PA-11500-18000-PS44p5T is a GaN HEMT MMIC power amplifier supplied as a bare die for the transmit path of microwave transceiver assemblies and solid-state transmitters. It covers 11.5–18 GHz and supports continuous-wave (CW) and pulsed operation.



At an ambient temperature of +25 °C with Vd = +28 V, Vg = −2.4 V and 25 dBm RF input, the published pulse test uses 100 µs pulses at 10% duty cycle. Under those conditions, saturated output power (Psat) is 44 dBm minimum and 44.5 dBm typical.

Typical large-signal power gain is 19.5 dB and typical power-added efficiency (PAE) is 30%. Use those conditions when comparing the ratings. They describe pulsed performance.

The 3.52 × 3.55 × 0.1 mm die uses backside vias for grounding. Both RF paths have integrated DC blocking, and both RF pads have a DC path to ground. The two gate pads are internally connected. Apply gate bias before drain bias on power-up and remove drain bias first on shutdown.

Use the pad layout and die outline to plan the assembly.

RF characteristics

TA = +25 °C; Vd = +28 V; Vg = -2.4 V; Pin = 25 dBm; τ = 100 µs; D = 10%

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating frequency	f	11500	-	18000	MHz
Saturated output power	Psat	44	44.5	-	dBm
Power gain	Gp	19	19.5	-	dB
Power-gain flatness	ΔGp	-	-	±0.5	dB
Power-added efficiency	PAE	28	30	-	%
Small-signal gain	S21	28	29	31	dB
Small-signal gain flatness	ΔS21	-	-	±1.5	dB
Input VSWR	VSWR(in)	-	1.8	2	-

DC bias and current

Parameter	Symbol	Minimum	Typical	Maximum	Value	Unit
Drain voltage	Vd	-	28	-	-	V
Gate voltage	Vg	-	-2.4	-	-	V
Quiescent drain current	Id	-	-	-	1.85 (Vd = +28 V; Adjustable; the source assigns no minimum, typical or maximum qualifier.)	A

Absolute limits

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Maximum drain-source voltage	Vd	-	-	32	V
Minimum gate bias	Vg	-5	-	-	V
Maximum input power	Pin	-	-	28	dBm
Storage temperature	TSTG	-65	-	150	°C
Maximum channel temperature	Top	-	-	200	°C

Die dimensions

Parameter	Value	Unit
Die dimensions	3.52 × 3.55 × 0.1	mm

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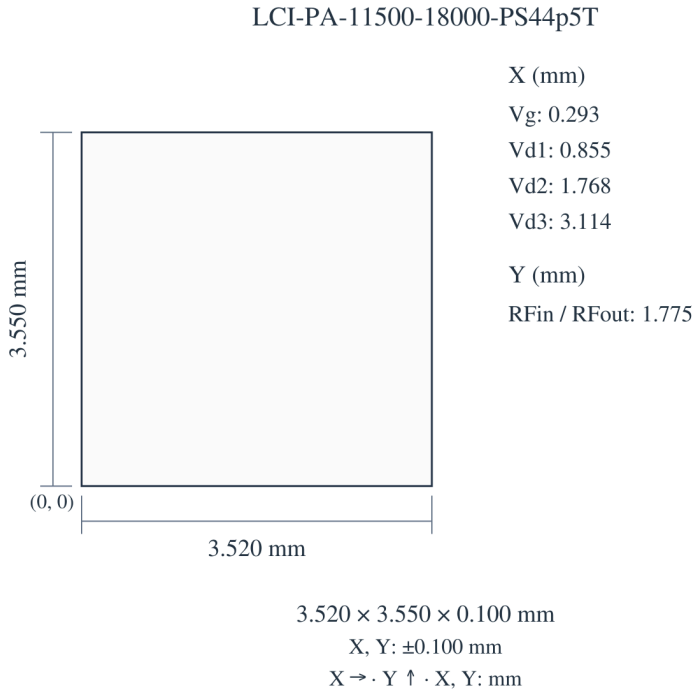
Die integration and bias sequencing

Integrated DC blocking: RFin / RFout. DC path to ground: RFin / RFout → GND. Internally connected gate pads: Vg ↔ Vg. Separate characterization: TA = +25 °C; Vd = +28 V; Vg = -2.4 V; Pin = 25 dBm; τ = 100 µs; D = 10%. Apply gate bias before drain bias. Remove drain bias before gate bias.

Mechanical Outline

Outline and dimensioned coordinates in mm. Use this drawing as a dimensional reference. Fabrication and wire bonding require complete drawings.

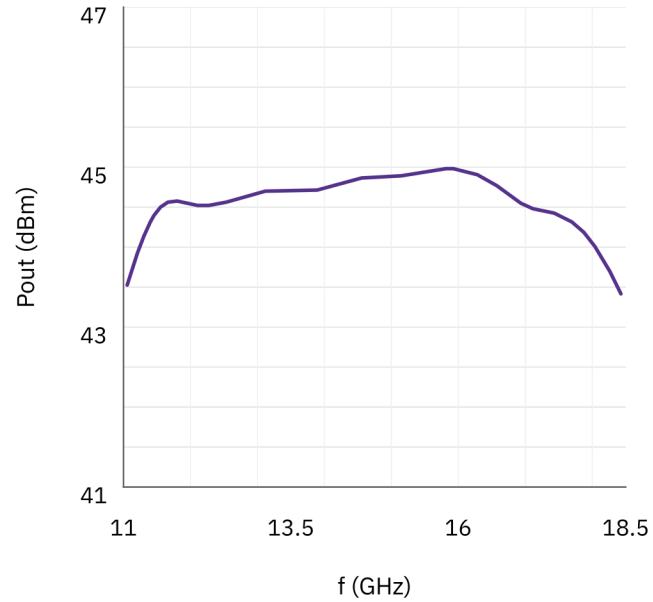


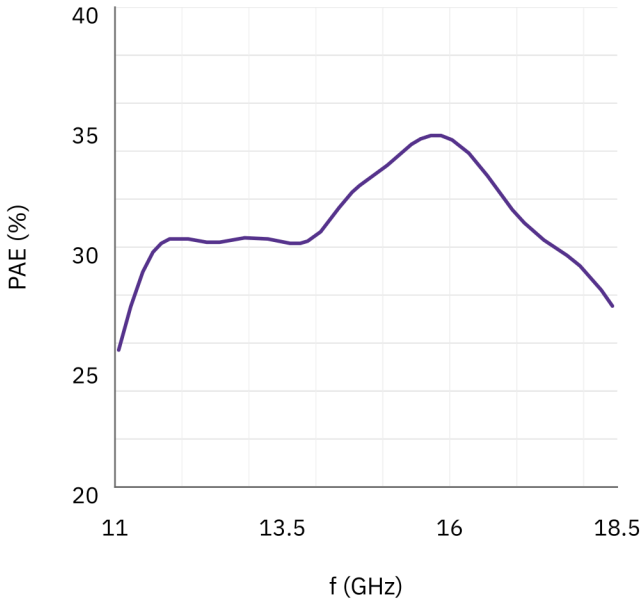
Performance curves

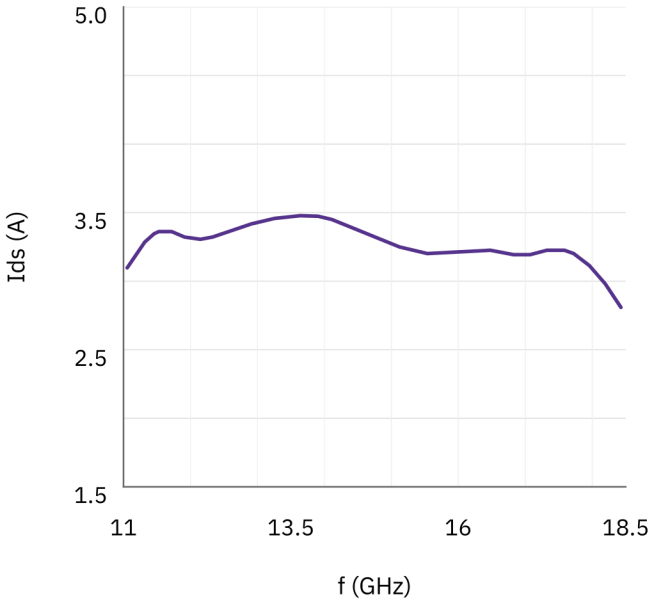
Each performance plot applies to its stated operating conditions.

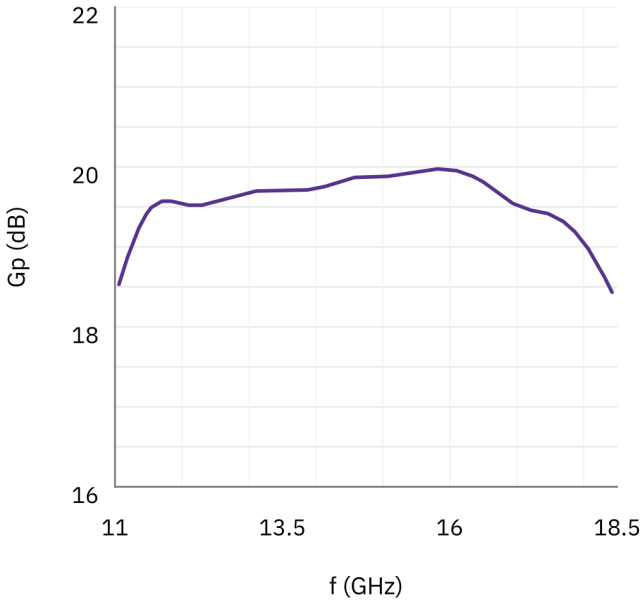
Pulsed — Saturated output power; Dynamic drain current; Power-added efficiency; Power gain.

Figure notes: TA=+25°C; Vd=+28V; Vg=-2.4V; Pin=25dBm. Pulse width = 100 µs; duty cycle = 10%. Readings are approximate.









Document notice

Specifications are subject to revision. Before design release, confirm the current document revision and product-specific requirements with LCRF. The approved quotation and order documentation define the supplied configuration.