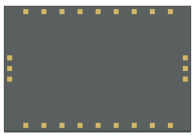
75000–110000 MHz GaAs MMIC Low-Noise Amplifier Die

LCI-LNA-75000-110000-NF3p3MAX — 75000–110000 MHz GaAs MMIC Low-Noise Amplifier Die.



Noise figure: 2.8 dB (typical) (f = 90000 MHz); Noise figure: 3.3 dB (maximum); Small-signal gain: 25 dB (typical) (f = 75000–90000 MHz); Small-signal gain: 22 dB (typical) (f = 90000–110000 MHz). Die dimensions: 2 × 3 × 0.1 mm.

RF characteristics

TA = +25 °C; VD1–VD4 = +1 V; VG1–VG4 = 0 V; IDtotal = 0.033 A

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating frequency	-	75000	-	110000	MHz
Small-signal gain [1]	-	-	25	-	dB
Small-signal gain [2]	-	-	22	-	dB
Input return loss	-	-	6	-	dB
Output return loss [1]	-	-	12	-	dB
Output return loss [2]	-	-	4	-	dB
Isolation [1]	-	-	35	-	dB
Output 1 dB compression power	-	-	1	-	dBm
Noise figure [3]	-	-	2.8	-	dB
Noise figure	-	-	-	3.3	dB

[1] f = 75000–90000 MHz

[2] f = 90000–110000 MHz

[3] f = 90000 MHz

DC bias and current

TA = +25 °C

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain voltage [1]	-	0.8	1	1.2	V
Gate voltage [2]	-	-0.1	0	0.1	V
Quiescent drain current [3]	-	-	0.033	-	A

[1] VD1–VD4

[2] VG1–VG4

[3] IDtotal = ID1 + ID2 + ID3 + ID4; ID1 = ID2 = ID3 = ID4; RF = 0

Absolute limits

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain voltage [1]	-	0	-	2	V
Maximum allowable current [2]	-	-	-	0.05	A
Gate voltage [3]	-	-2	-	0.6	V
Maximum junction temperature	-	-	-	150	°C

[1] VD1–VD4
[2] IDtotal
[3] VDx = Hi-Z

Environmental specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Storage temperature	-	-55	-	150	°C
Ambient temperature	-	-10	-	85	°C

Bond-pad assignments

Pins	Symbol
1	GND
2	RFIN
3	GND
4	NC
5	GND
6	VD1
7	VD2
8	GND
9	GND
10	VD3
11	GND
12	VD4
13	GND
14	RFOUT
15	GND
16	VG1

Bond-pad assignments

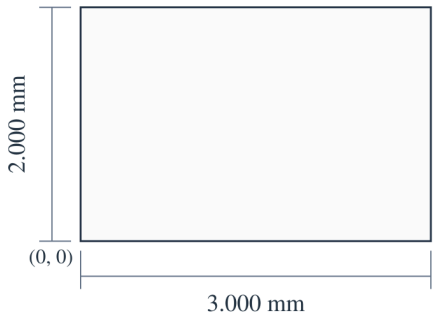
Pins	Symbol
17	GND
18	VG2
19	GND
20	GND
21	VG3
22	GND
23	VG4
24	NC

Die dimensions

Parameter	Value	Unit
Die dimensions	2 × 3 × 0.1	mm

Outline and dimensioned coordinates in mm. Use this drawing as a dimensional reference. Fabrication and wire bonding require complete drawings.

LCI-LNA-75000-110000-NF3p3MAX



3.000 × 2.000 × 0.100 mm
X, Y: ±0.015 mm
X → · Y ↑ · X, Y: mm

Current publication record · 1.8 · 2026-11-12. Product description or editorial content updated. Replaces revision 1.7.

Die integration and bias sequencing

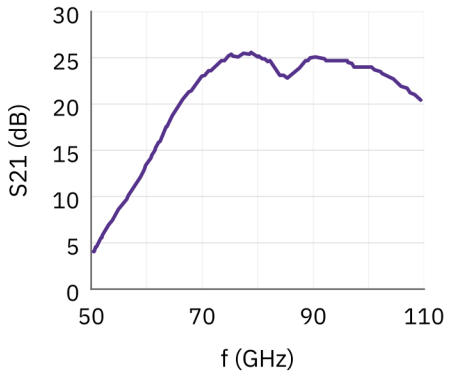
Values are based on on-wafer RF measurements. Set VG1–VG4 to −1 V, then raise all VD to +1 V while monitoring current. Adjust the gate biases to IDtotal = 0.033 A without an RF signal, then apply RF. External supply decoupling capacitors to ground are required.

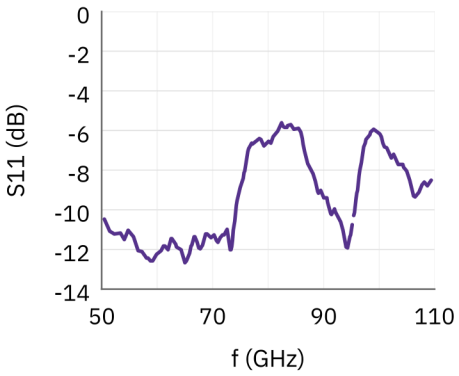
Performance curves

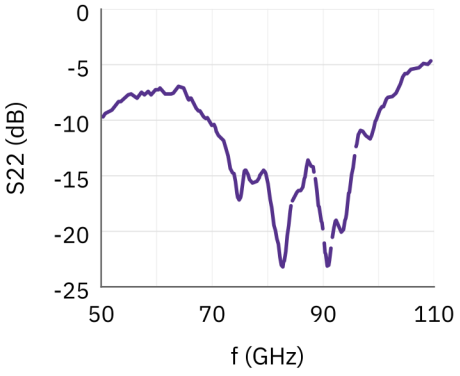
Each performance plot applies to its stated operating conditions.

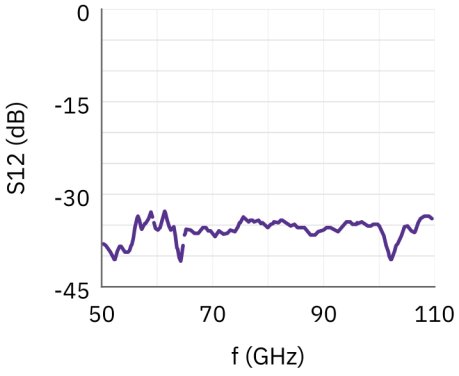
Small-signal gain; Noise figure; Input matching; Output matching; Reverse isolation.

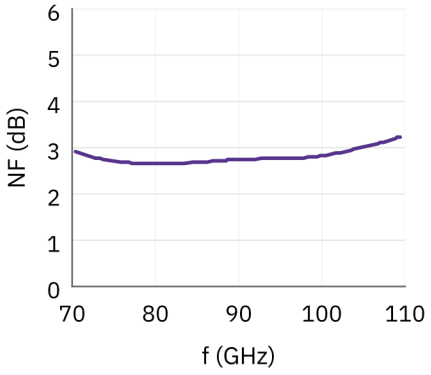
Figure notes: TA=+25°C; VD = 1 V; VG = 0 V. Readings are approximate. TA = +25 °C; VD = 1 V; VG = 0 V; IDtotal = 33 mA. On-wafer test; IDtotal is total drain current, not Idq. S21 / S11 / S22 / S12 (dB); NF (dB).





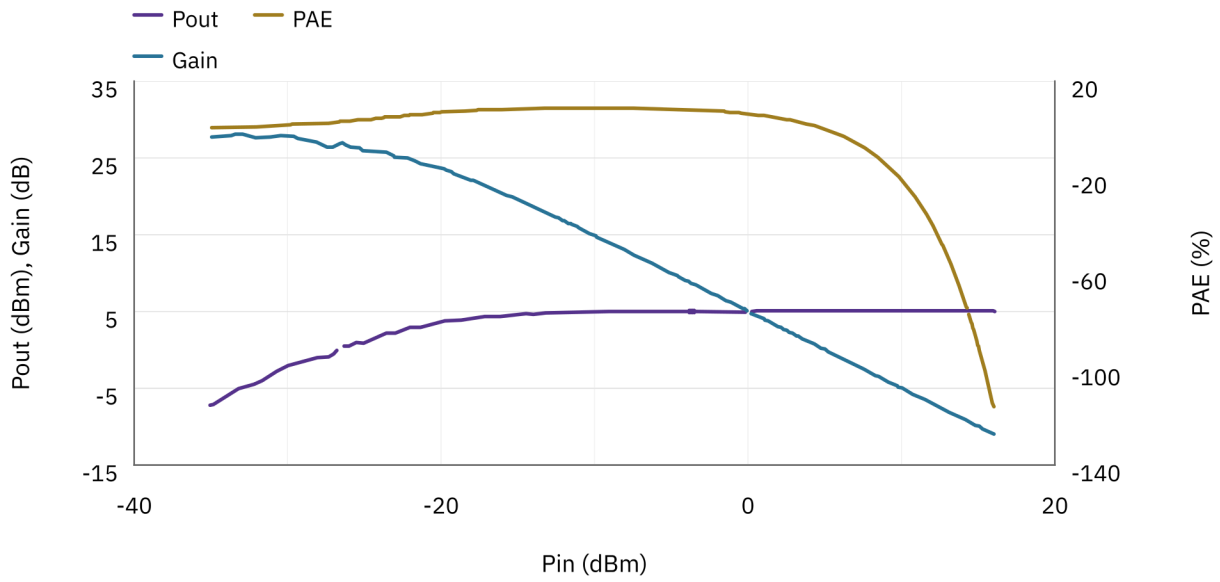


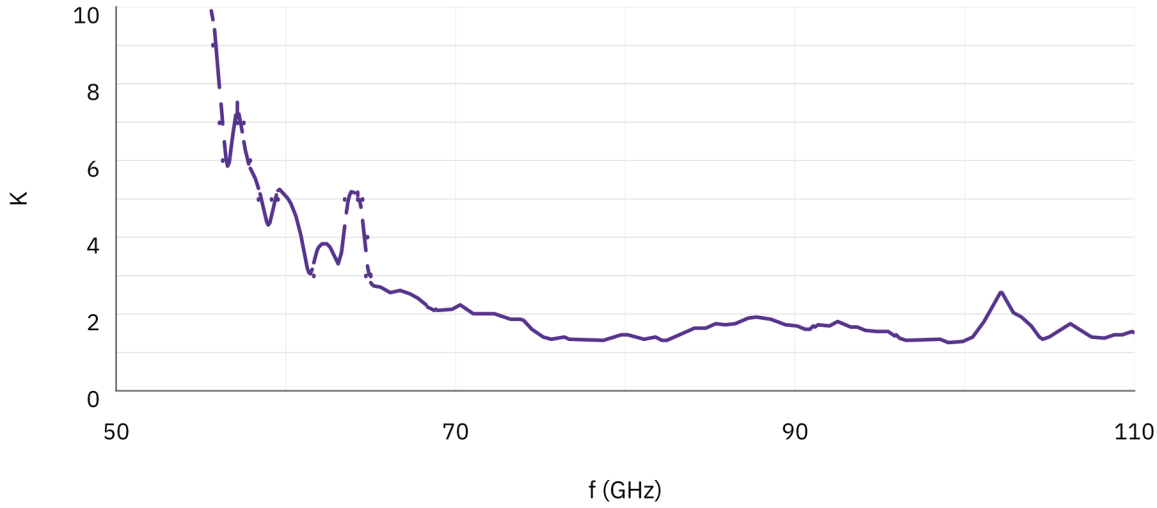




Output power; Power gain; Power-added efficiency; Stability factor.

Readings are approximate. Reference plot at 90 GHz: Pout, gain and PAE versus Pin. PAE includes negative values. The characterization method and bias conditions are unspecified for this plot.





Document notice

Specifications are subject to revision. Before design release, confirm the current document revision and product-specific requirements with LCRF. The approved quotation and order documentation define the supplied configuration.