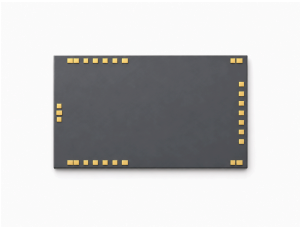
3700–5000 MHz Dual-Channel GaAs MMIC Phase and Attenuation Control Die — 2 × 6-bit φ / 6-bit ATT



LCI-BF-3700-5000-2CH · 3700–5000 MHz · Dual-Channel GaAs MMIC Phase and Attenuation Control Die.

The RF table specifies: Insertion loss -13 dB (typical); 64-state RMS attenuation error 0.2 dB (typical); 64-state RMS phase error 2 ° (typical). RF test conditions: TA = +25 °C; VEE = -5 V; Vd = +5 V.

27-bit serial TTL control sends D1 first and D27 last. Each RF branch has 6-bit phase and 6-bit attenuation control.

Die dimensions: 5 × 3 × 0.1 mm.

RF1 φ: D16..D21:5.625,11.25,22.5,45,90,180°

RF1 ATT: D22..D27:0.5,1,2,4,8,16dB

RF2 φ: D12..D7:5.625,11.25,22.5,45,90,180°

RF2 ATT: D6..D1:0.5,1,2,4,8,16dB

ST1: D15

ST2: D14

ST3: D13

ST4: D13 ∨ D14 ∨ D15

RF characteristics

TA = +25 °C; VEE = -5 V; Vd = +5 V

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating frequency	f	3700	-	5000	MHz
Insertion loss	-	-	-13	-	dB
Attenuation range	-	-	-	31.5	dB
64-state RMS attenuation error	-	-	0.2	-	dB
Attenuation-induced phase variation	-	-	-	±3	°
Phase shift range	-	-	-	354.375	°
64-state RMS phase error	-	-	2	-	°
Phase-induced amplitude variation	-	-	±0.5	-	dB
Input VSWR	-	-	1.5	-	-
Output VSWR	-	-	1.3	-	-
Negative-supply quiescent current (RF)	-	-	-	0.014	A

DC bias and current

TA = +25 °C

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Negative supply voltage	-	-5.3	-5	-4.7	V
Positive supply voltage	-	4.7	5	5.3	V
Negative-supply quiescent current	-	-	-	0.01	A
Positive-supply quiescent current	-	-	-	0.001	A
Input drive current [1]	-	-	0.0002	-	A
High-level input voltage	-	3	-	5	V
Low-level input voltage	-	0	-	0.4	V
Clock frequency	-	-	-	10	MHz

[1] TTL = +5 V; LD / DAT / CLK

Absolute limits

Absolute limits; these are not normal operating targets.

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Maximum input power	-	-	-	20	dBm
Storage temperature	-	-65	-	150	°C
Operating temperature	-	-55	-	85	°C
Minimum negative supply voltage	-	-6	-	-	V
Maximum operating voltage	-	-	-	6	V
Maximum input drive current	-	-	-	0.0003	A

Die dimensions

Parameter	Value	Unit
Die dimensions	5 × 3 × 0.1	mm
Plan-view outline tolerance	±50	µm

Bond-pad assignments

Pins	Symbol	mm
1	GND	0.100 × 0.100
2	COM	0.150 × 0.100
3	GND	0.100 × 0.100

Bond-pad assignments

Pins	Symbol	mm
4	GND	0.150 × 0.100
5	Vd	0.150 × 0.100
6	ST4	0.100 × 0.100
7	ST3	0.150 × 0.100
8	ST2	0.100 × 0.100
9	ST1	0.100 × 0.100
10	—	0.150 × 0.100
11	GND	0.100 × 0.100
12	RF1	0.150 × 0.100
13	GND	0.100 × 0.100
14	VEE	0.150 × 0.100
15	CS	0.150 × 0.100
16	CLK	0.150 × 0.100
17	DAT	0.150 × 0.100
18	LD	0.150 × 0.100
19	Vd	0.100 × 0.100
20	RF2	0.150 × 0.100
21	GND	0.100 × 0.100
22	—	0.150 × 0.100
23	ST1	0.100 × 0.100
24	ST2	0.100 × 0.100
25	ST3	0.150 × 0.100
26	ST4	0.100 × 0.100
27	Vd	0.150 × 0.100
28	GND	0.150 × 0.100

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Integration notes

27-bit serial TTL control sends D1 first and D27 last. Each RF branch has 6-bit phase and 6-bit attenuation control. RF1 φ: D16..D21:5.625,11.25,22.5,45,90,180° RF1 ATT: D22..D27:0.5,1,2,4,8,16dB RF2 φ: D12..D7:5.625,11.25,22.5,45,90,180° RF2 ATT: D6..D1:0.5,1,2,4,8,16dB ST1: D15 ST2: D14 ST3: D13 ST4: D13 ∨ D14 ∨ D15

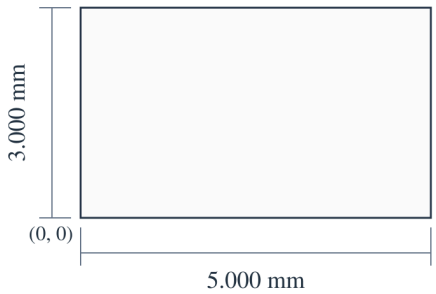
Pad connection notes

Reference state: D1–D27 = 0. ST1 / ST2 / ST3 / ST4: TTL. Vd (5, 19, 27) = +5 V; VEE (14) = −5 V. CS / CLK / DAT / LD: LVTTL / TTL. 0 = 0 V; 1 = +3.3 / +5 V.

Mechanical Outline

Outline and dimensioned coordinates in mm. Use this drawing as a dimensional reference. Fabrication and wire bonding require complete drawings.

LCI-BF-3700-5000-2CH



X (mm)
4 / 28: 0.450
5 / 27: 0.600
6 / 26: 0.850
7 / 25: 1.100
8 / 24: 1.350
9 / 23: 1.600
10 / 22: 1.850
12: 4.850

Y (mm)
COM: 1.500

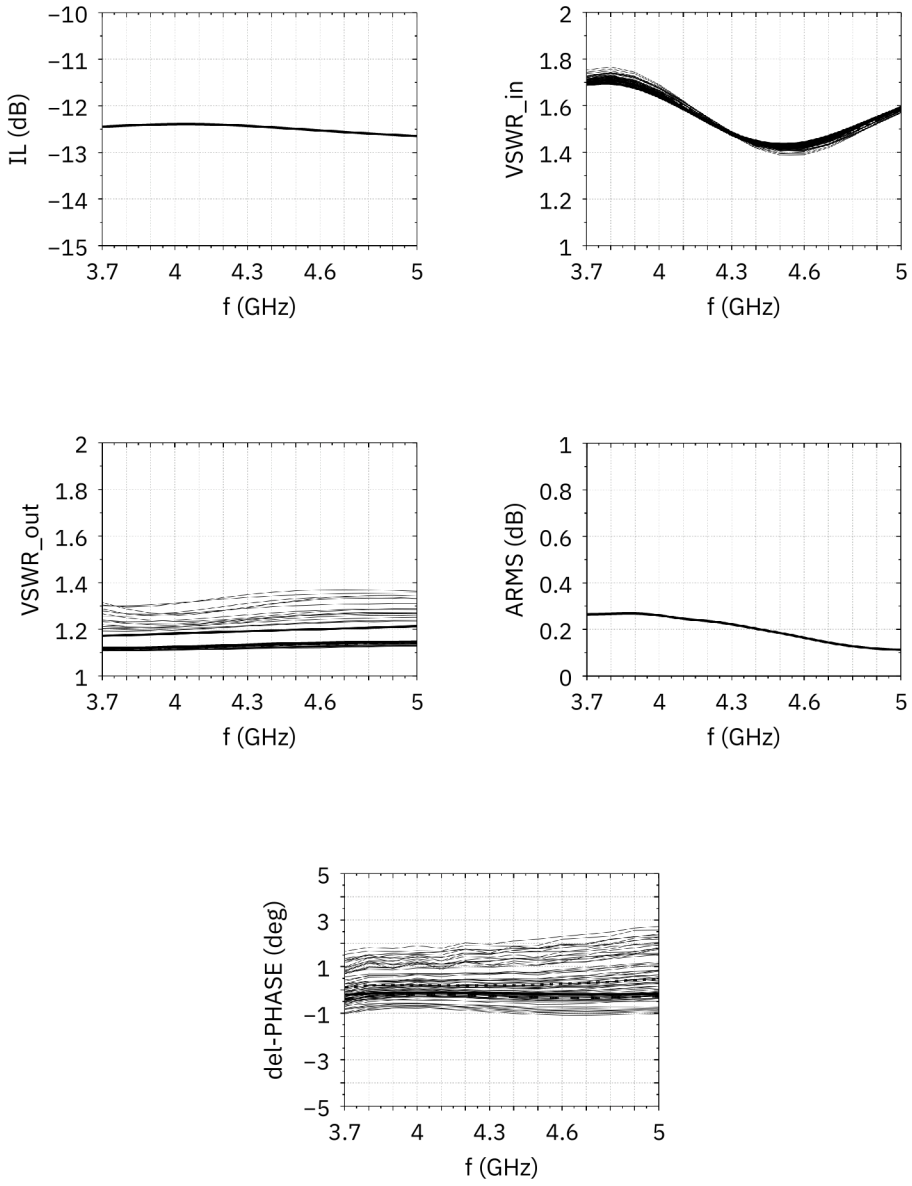
5.000 × 3.000 × 0.100 mm
X, Y: ±0.050 mm
X → · Y ↑ · X, Y: mm

Performance curves

Each performance plot applies to its stated operating conditions.

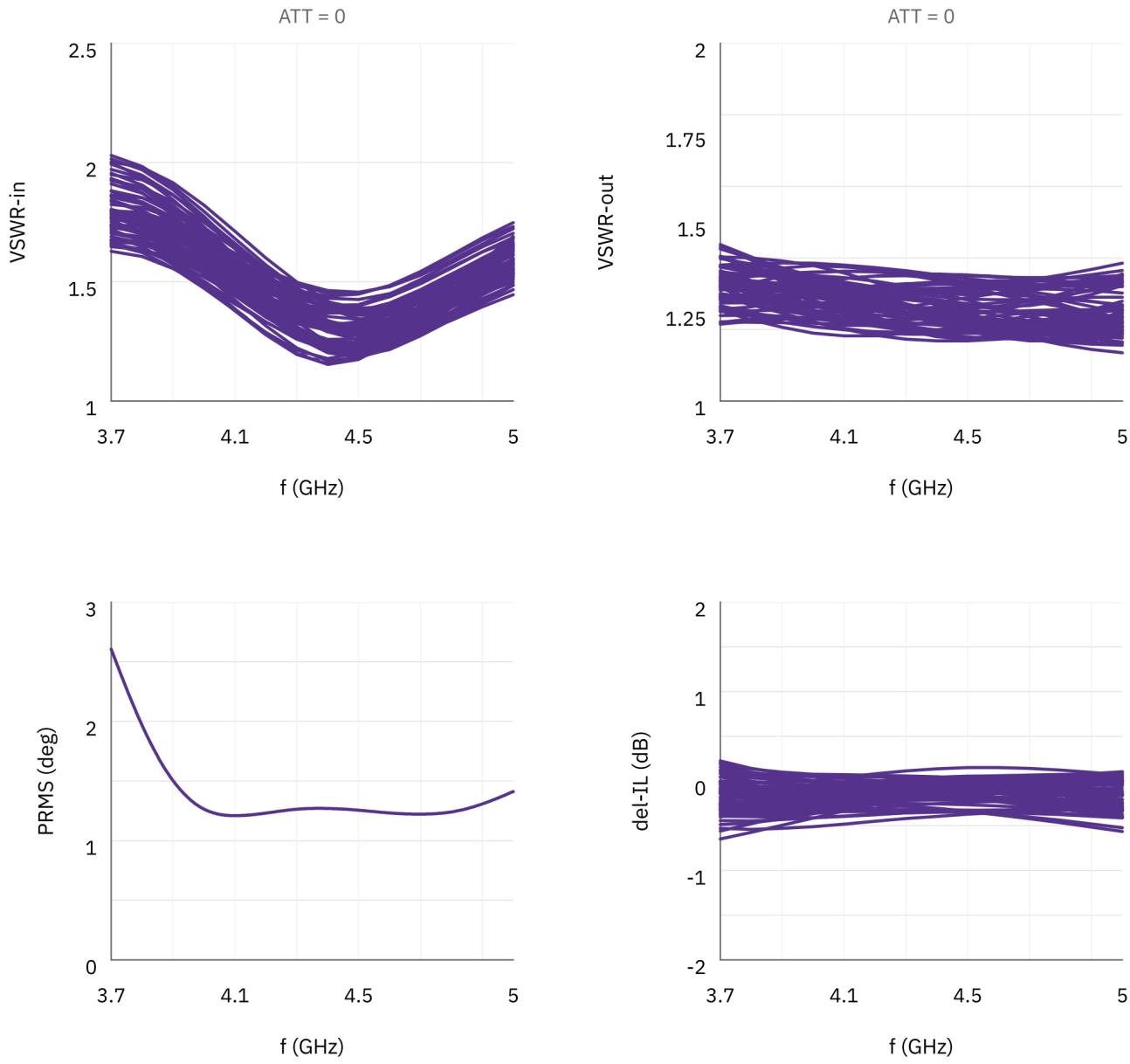
Insertion loss; Input matching; Output matching; 64-state RMS attenuation error; Attenuation-induced phase variation.

Figure notes: Input and output VSWR apply to the phase-zero state. RMS attenuation error and attenuation-induced phase variation cover 64 attenuation states.



Input matching; Output matching; 64-state RMS phase error; Phase-induced amplitude variation.

Readings are approximate. VSWR-in/VSWR-out: ATT = 0.



Document notice

Specifications are subject to revision. Before design release, confirm the current document revision and product-specific requirements with LCRF. The approved quotation and order documentation define the supplied configuration.