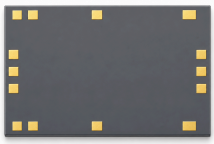
24000–31000 MHz GaAs MMIC Amplifier Die — PSAT 25 dBm (typical)

LCI-AMP-24000-31000-PS25T · 24000–31000 MHz · GaAs MMIC Amplifier Die.



The RF table specifies: PSAT 25 dBm (typical); Small-signal gain 22 dB (typical). RF test conditions: TA = +25 °C; Vd = +5 V; Id = 160 mA.

Input and output DC-blocking capacitors are integrated.

The RF pads do not require external DC-blocking capacitors; add the specified supply filtering at VDD.

VD1 / VD2 / VD3 / VD4; VG1 / VG2

Apply gate bias before drain bias. Remove drain bias before gate bias.

Die dimensions: 2.25 × 1.6 × 0.07 mm.

RF characteristics

TA = +25 °C; Vd = +5 V; Id = 160 mA

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating frequency	f	24000	-	31000	MHz
Small-signal gain	-	-	22	-	dB
Saturated output power	-	-	25	-	dBm
Power gain	-	-	20	-	dB
Power-gain flatness	-	-	±1	-	dB
Power-added efficiency	-	-	30	-	%
Small-signal gain flatness	-	-	±0.3	-	dB
Input/output VSWR	-	-	1.3	-	-
Current at saturation	-	-	-	0.23	A

DC bias and current

Vd = +5 V; Vg = -0.45 V

Parameter	Symbol	Minimum	Typical	Maximum	Value	Unit
Operating voltage	-	-	-	-	5	V
Quiescent current	-	-	-	-	0.16 (Vg = -0.45 V)	A
Gate voltage	-	-	-	-	-0.45	V

Absolute limits

Absolute limits; these are not normal operating targets.

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Maximum operating voltage	-	-	-	6	V
Maximum input power	-	-	-	10	dBm
Storage temperature	-	-65	-	150	°C

Absolute limits

Absolute limits; these are not normal operating targets.

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating temperature	-	-55	-	85	°C
Minimum gate bias	-	-5	-	-	V
Maximum channel temperature	-	-	-	175	°C

Die dimensions

Parameter	Value	Unit
Die dimensions	2.25 × 1.6 × 0.07	mm
Plan-view outline tolerance	±50	µm

Bond-pad assignments

Pins	Symbol	mm
1	RFI	0.090 × 0.110
2	RFO	0.090 × 0.110
3	VG1	0.100 × 0.100
4	VG2	0.100 × 0.100
5	VD1	0.120 × 0.100
6	VD3	0.120 × 0.100
7	VD2	0.150 × 0.100
8	VD4	0.150 × 0.100

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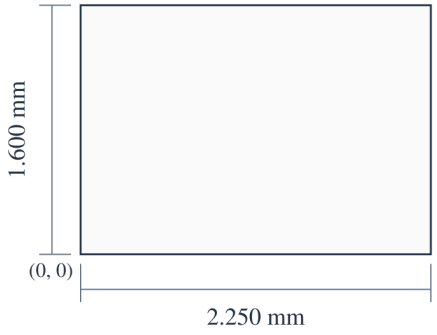
Integration notes

Input and output DC-blocking capacitors are integrated. The RF pads do not require external DC-blocking capacitors; add the specified supply filtering at VDD. VD1 / VD2 / VD3 / VD4; VG1 / VG2 Apply gate bias before drain bias. Remove drain bias before gate bias.

Mechanical Outline

Outline and dimensioned coordinates in mm. Use this drawing as a dimensional reference. Fabrication and wire bonding require complete drawings.

LCI-AMP-24000-31000-PS25T



X (mm)
VG1 / VG2: 0.320
VD1 / VD3: 1.010
VD2 / VD4: 2.000

Y (mm)
RFI / RFO: 0.800

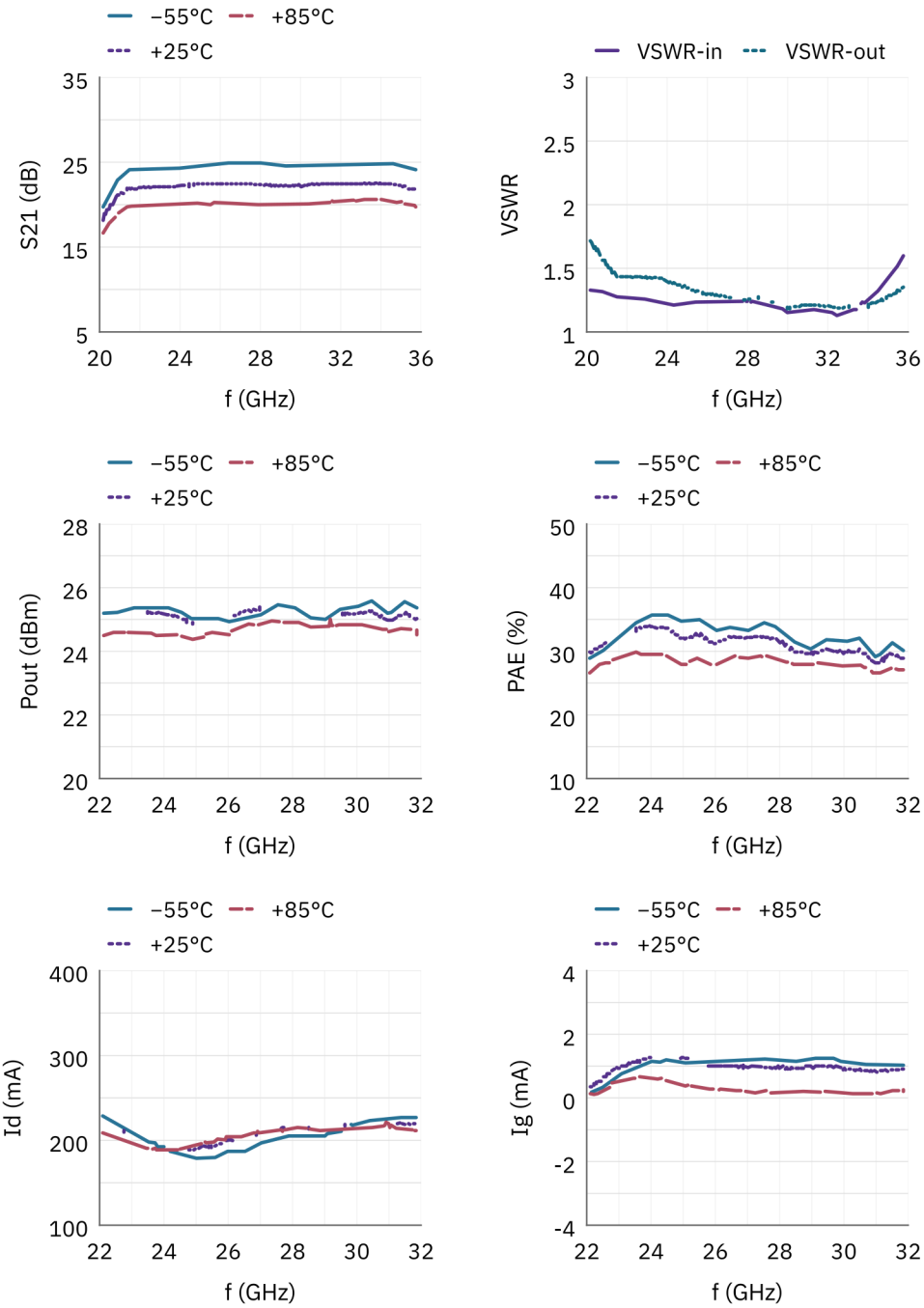
2.250 × 1.600 × 0.070 mm
X, Y: ±0.050 mm
X → · Y ↑ · X, Y: mm

Performance curves

Each performance plot applies to its stated operating conditions.

Continuous wave (CW) — Small-signal gain; Input matching; Output matching; Output power; Power-added efficiency; Drain current; Gate current.

Figure notes: TA=+25°C; Vd=5V; Id=160mA. Readings are approximate. Pout / PAE / Id / Ig: Pin = 5 dBm. Use the operating conditions in each trace's legend.



Document notice

Specifications are subject to revision. Before design release, confirm the current document revision and product-specific requirements with LCRF. The approved quotation and order documentation define the supplied configuration.